

Defect oriented fault coverage of 100stuck-at fault test sets

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 511-516 : ill <https://repo.pw.edu.pl/info/seam?ps=20&id=WUT7e20f35d67ae45d3b2d1264d7a4ba722?en&pn=1&cid=156607>

Defect-oriented fault simulation and test generation in digital circuits

Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE ISQED 2001 : proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design : March 26-28, 2001, San Jose, California 2001 / p. 365-371 <https://ieeexplore.ieee.org/document/915257>

Defect-oriented library builder and hierarchical test generation

Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 163-168 : ill

Defect-oriented test generation and fault simulation in the environment of MOSCITO

Schneider, Andre; Diener, Karl-Heinz; Gramatova, Elena; Fisherova, Maria; **Ivask, Eero; Ubar, Raimund-Johannes**; Pleskacz, Witold A.; Kuzmich, W. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 303-306 : ill

Defect-oriented test generation using probabilistic estimation

Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 131-136 : ill

Hierarchical defect level test quality analysis

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE European Test Workshop : 23-26 May 2000, Cascais, Portugal : ETW 2000 : proceedings 2000 / p. 69-74 : ill <https://ieeexplore.ieee.org/document/873781>

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmich, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE European Test Workshop 2000 / p. 151-156 <https://ieeexplore.ieee.org/document/873781>

Hierarchical test generation for combinational circuits with real defects coverage

Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Microelectronics reliability 2002 / p. 1141-1149 : ill <https://www.sciencedirect.com/science/article/pii/S002627140200080X>

Probabilistic analysis of CMOS physical defects in VLSI circuits for test coverage improvement

Blyzniuk, M.; Kazymyra, I.; Kuzmich, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** Microelectronics reliability 2001 / p. 2023-2040 : ill <https://www.sciencedirect.com/science/article/pii/S0026271401000920>

Virtual laboratory for research in dependable microelectronics

Diener, Karl-Heinz; Elst, G.; Gramatova, Elena; Kuzmich, W.; Peng, Z.; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 217-220 : ill