

Chip-to-Chip authentication method based on SRAM PUF and public key cryptography

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From virtual characterization to test-chips : DFM analysis through pattern enumeration

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Latch-Based logic locking

Sweeney, J.; Mohammed Zackriya, V.; **Pagliarini, Samuel Nascimento**; Pileggi, Larry Proceedings of the IEEE International Symposium on Hardware Oriented Security and Trust, HOST 2020 2020 / p. 132–141 : ill <https://doi.org/10.1109/HOST45689.2020.9300256>

Logic IP for low-cost IC design in advanced CMOS nodes

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A probabilistic synapse with strained MTJs for Spiking Neural Networks

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Split-chip design to prevent IP reverse engineering

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