

From FPGAs to obfuscated eASICs : design and security trade-offs

Abideen, Zain Ul; Perez, Tiago Diadami; Pagliarini, Samuel Nascimento IEEE Asian Hardware-Oriented Security and Trust (AsianHOST) 2021 / p. 1-4 <https://doi.org/10.1109/AsianHOST53231.2021.9699758>

Hardware obfuscation of digital FIR filters

Aksoy, Levent; Hepp, Alexander; Baehr, Johanna; **Pagliarini, Samuel Nascimento** 2022 25th International Symposium on Design and Diagnostics of Electronic Circuits and Systems (DDECS) : Prague, Czech Republic : April 6-8, 2022 : proceedings 2022 / p. 68-73 <https://doi.org/10.48550/arXiv.2202.10022> <https://doi.org/10.1109/DDECS54261.2022.9770141>

High-level intellectual property obfuscation via decoy constants

Aksoy, Levent; Nguyen, Quang-Linh; **Almeida, Felipe; Raik, Jaan;** Flottes, Marie-Lise; Dupuis, Sophie; **Pagliarini, Samuel Nascimento** 2021 IEEE 27th International Symposium on On-Line Testing and Robust System Design (IOLTS) : Torino, Italy, 28-30 June 2021 2021 / p. 1-7 <https://doi.org/10.1109/IOLTS52814.2021.9486714>

Hybrid protection of digital FIR filters

Aksoy, Levent; Nguyen, Quang-Linh; **Almeida, Felipe; Raik, Jaan;** Flottes, Marie-Lise; Dupuis, Sophie; **Pagliarini, Samuel Nascimento** IEEE transactions on Very Large Scale Integration (VLSI) Systems 2023 / p. 812-825 : ill <https://doi.org/10.1109/TVLSI.2023.3253641> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

A security-aware and LUT-based CAD flow for the physical synthesis of hASICs

Abideen, Zain Ul; Perez, Tiago Diadami; Martins, Mayler; **Pagliarini, Samuel Nascimento** IEEE transactions on computer-aided design of integrated circuits and systems 2023 / p. 3157-3170 : ill <https://doi.org/10.1109/TCAD.2023.3244879> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)