Application specific true critical paths identification in sequential circuits
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan**; **Devadze, Sergei**; **Oyeniran, Adeboye Stephen** 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 299-304 : ill https://doi.org/10.1109/IOLTS.2019.8854442

Architectural solutions for high-speed data processing demands of CERN LHC detectors with FPGA and high-level synthesis
Devadze, Sergei; Nielsen, Christine Elizabeth; **Mihhailov, Dmitri**; **Ellervee, Peeter** 2024 IEEE Nordic Circuits and Systems Conference (NorCAS) 2024 https://doi.org/10.1109/NorCAS64408.2024.10752490 Article at Scopus

Asynchronous fault detection in IEEE P1687 instrument network
Shibin, Konstantin; **Devadze, Sergei**; **Jutman, Artur** IEEE 23rd North Atlantic Test Workshop : 14-16 May 2014, Binghampton, New York : proceedings 2014 / p. 73-78 : ill

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Devadze, Sergei**; **Raik, Jaan**; **Min, Mart** 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

Automatic SoC level test path synthesis based on partial functional models
Tšertov, Anton; **Ubar, Raimund-Johannes**; **Jutman, Artur**; **Devadze, Sergei** 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 https://ieeexplore.ieee.org/document/6114730

Automation of testing beyond the SoCs
Tšertov, Anton; **Jutman, Artur**; **Devadze, Sergei** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 29-32 : ill

BASTION - board and SoC test instrumentation for Ageing and No Failure Found
Devadze, Sergei MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 77

A benchmark suite for evaluating the efficiency of test tools
Kruus, Helena; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Gorev, Maksim**; **Pesonen, Vadim**; **Devadze, Sergei**; **Orasson, Elmet**; **Brik, Marina**; **Min, Mart**; **Annus, Paul**; **Kruus, Margus**; **Meigas, Kalju** BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 85-88 : ill

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
http://icee2007.dei.uc.pt/proceedings/papers/429.pdf

CMS drift tubes sector collector relocation phase 1 upgrade [Electronic resource]
Bedoya, C. F.; **Jutman, Artur**; **Shibin, Konstantin**; **Devadze, Sergei** 2015 http://cms.cern.ch/iCMS/jsp/openfile.jsp?type=DN&year=2015&files=DN2015_011.pdf

Collaborative distributed computing in the field of digital electronics testing
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Balanced Automation Systems for Future Manufacturing Networks : 9th IFIP WG 5.5 International Conference : BASYS 2010 : Valencia, Spain, July 21-23, 2010 : proceedings 2010 / p. 145-152

Collaborative distributed fault simulation for digital electronic circuits
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Intelligent Distributed Computing IV : proceedings of the 4th International Symposium on Intelligent Distributed Computing - IDC 2010 : Tangier, Morocco, September 2010 2010 / p. 67-76

Combinational fault simulation in sequential circuits
Ubar, Raimund-Johannes; **Kõusaar, Jaak**; **Gorev, Maksim**; **Devadze, Sergei** 2015 IEEE International Symposium on Circuits and Systems : 24-27 May 2015, Lisboa, Portugal : [proceedings] 2015 / p. 2876-2879 : ill https://doi.org/10.1109/ISCAS.2015.7169287 Conference proceedings at Scopus Article at Scopus Article at WOS

Computer aided design support of FSM multiplicative decomposition
Sudnitsõn, Aleksander; **Devadze, Sergei** Proceedings of the IEEE East-West Design & Test Workshop (EWDTW'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 241-246 : ill

Critical path tracing based simulation of transition delay faults
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 61-66 : ill

Critical path tracing based simulation of transition delay faults
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 108-113 : ill

DefSim - the defective IC
Pleskacz, Witold A.; **Jutman, Artur**; **Ubar, Raimund-Johannes**; **Devadze, Sergei** DATE 2007 : Design Automation and Test in Europe : Nice, France, April 16-20, 2007 2007 / p. s96 (2 p.)

Designing reliable cyber-physical systems
Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei**; **Jenihhin, Maksim**; **Jutman, Artur**; **Raik, Jaan**; **Shibin, Konstantin** Languages, design methods, and tools for electronic system design : selected contributions from FDL 2016 2018 / p. 15-38 : ill https://doi.org/10.1007/978-3-319-62920-9_2 Conference Proceedings at Scopus Article at Scopus

Designing reliable cyber-physical systems : overview associated to the special session at FDL'16
Aleksandrowicz, Gadi; Arbel, Eli; Bloem, Roderick; **Devadze, Sergei**; **Jenihhin, Maksim**; **Jutman, Artur**; **Raik, Jaan**; **Shibin, Konstantin** The 2016 Forum on Specification & Design Languages : proceedings : Bremen, Germany, September 14-16, 2016 2016 / [8] p. : ill https://doi.org/10.1109/FDL.2016.7880382

Digital logic simulation with compressed BDDs
Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Devadze, Sergei**; **Raik, Jaan** Proceedings : 2011 IEEE International Conference on Computer Science and Automation Engineering : June 10-12, 2011, Shanghai, China 2011 / p. 105-109 : ill https://ieeexplore.ieee.org/document/5952643

Distributed approach for parallel exact critical path tracing fault simulation
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** MIXDES 2010 : 17th International Conference "Mixed Design of Integrated Circuits and Systems" : June 24-26, 2010, Wroclaw, Poland 2010 / p. 471-476 : ill

Distributed approach for parallel exact critical path tracing fault simulation
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** International journal of microelectronics and computer science 2010 / p. 165-174 : ill

Distributed fault simulation with collaborative load balancing for VLSI circuits
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Scalable computing : practice and experience 2011 / p. 153-163 : ill

Effective scalable IEEE 1687 instrumentation network for fault management
Jutman, Artur; **Shibin, Konstantin**; **Devadze, Sergei** IEEE design & test 2013 / p. 26-35 : ill https://doi.org/10.1109/MDAT.2013.2278535 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Efficient single-pattern fault simulation on structurally synthesized BDDs
Raik, Jaan; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Jutman, Artur** Dependable Computing - EDCC-5 : 5th European Dependable Computing Conference : Budapest, Hungary, April 20-22, 2005 : proceedings 2005 / p. 332-344 : ill

E-learning environment for WEB-based study of testing
Ubar, Raimund-Johannes; **Jutman, Artur**; **Raik, Jaan**; **Devadze, Sergei**; **Jenihhin, Maksim**; **Aleksejev, Igor**; **Tšepurov, Anton**; **Tšertov, Anton**; **Kostin, Sergei**; **Orasson, Elmet**; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 2010 / p. 47-52 : ill

E-learning tools for digital test
Devadze, Sergei; Gorjachev, R.; **Jutman, Artur**; **Orasson, Elmet**; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** Proc. III International Conference "Distance Learning - Educational Sphere of XXI Century" : Minsk, Belorussia, 2003 2003 / p. 336-342

Embedded instrumentation toolbox for screening marginal defects and outliers for production
Odintsov, Sergei; Jutman, Artur; Devadze, Sergei; **Aleksejev, Igor** IEEE AUTOTESTCON 2017 : Schaumburg, USA, Sept 11-14, 2017 : proceedings 2017 / p. 336-334 : ill https://doi.org/10.1109/AUTEST.2017.8080516

Embedded synthetic instruments for board-level testing
Jutman, Artur; **Devadze, Sergei**; **Aleksejev, Igor**; Wenzel, Thomas Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p. : ill https://ieeexplore.ieee.org/document/6233044

Environment for the analysis of functional self-test quality in digital systems
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Kruus, Helena**; **Aarna, Margit**; **Devadze, Sergei** Proceedings of the Estonian Academy of Sciences 2014 / p. 151-162 : ill https://artiklid.elnet.ee/record=b2673964*est https://doi.org/10.3176/proc.2014.2.05 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Exact parallel critical path fault tracing to speed-up fault simulation in sequential circuits
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Kostin, Sergei**; **Devadze, Sergei**; **Raik, Jaan** International journal of microelectronics

and computer science 2018 / p. 9−18 https://ijmcs.dmcs.pl/web/guest/vol.-9-no.-1
https://ijmcs.dmcs.pl/documents/10630/345460/IJMCS_1_2018_2.pdf

Fast extended test access via JTAG and FPGAs
Devadze, Sergei; **Jutman, Artur**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes** International Test Conference 2009 : November 1 - November 6, 2009, Austin Convention Center, Austin, Texas USA : proceedings 2009 / p. 1-7 : ill
http://dx.doi.org/10.1109/TEST.2009.5355668

Fast fault simulation for extended class of faults in scan-path circuits
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** Proceedings : Fifth IEEE International Symposium on Electronic Design, Test and Applications : DELTA 2010 : 13-15 January 2010, Ho Chi Minh City, Vietnam 2010 / p. 14-19
https://ieeexplore.ieee.org/document/5438717

Fault management instrumentation network based on IEEE P1687 IJTAG
Shibin, Konstantin; **Jutman, Artur**; **Devadze, Sergei** European Test Symposium (ETS), 2013, Avignon, France 2013

Fault simulation of digital systems = Digitaalsüsteemide rikete simuleerimine
Devadze, Sergei 2009 https://digi.lib.ttu.ee/i/?445 https://www.ester.ee/record=b2508727*est

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs
Devadze, Sergei; **Raik, Jaan**; **Jutman, Artur**; **Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

Fault simulation with parallel exact critical path tracing in multiple core environment
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Devadze, Sergei** 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2015 / p. 1180-1185 : ill

FPGA-based embedded virtual instrumentation = FPGA-sisesed virtuaalsed test- ja mõõtevahendid
Aleksejev, Igor 2013 http://www.ester.ee/record=b2927687*est

FPGA-based synthetic instrumentation for board test
Aleksejev, Igor; **Jutman, Artur**; **Devadze, Sergei**; **Odintsov, Sergei**; Wenzel, Thomas Proceedings : International Test Conference 2012 2012 / p. 1-10 : ill https://ieeexplore.ieee.org/document/6401571

FSM decomposition software for education and research
Devadze, Sergei; **Sudnitsõn, Aleksander** Proc. IEEE EUROCON 2005 International Conference on Computer as a tool : Belgrade, Serbia & Montenegro 2005 / p. 839-842 https://ieeexplore.ieee.org/document/1630063

Functional self-test of high-performance pipe-lined signal processing architectures
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Devadze, Sergei**; **Raik, Jaan**; **Min, Mart** Microprocessors and microsystems 2015 / p. 909-918 : ill https://doi.org/10.1016/j.micpro.2014.11.002 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Hardware/Software co-design in practice : MEMOCODE'08 contest experience
Reinsalu, Uljana; **Devadze, Sergei**; **Jutman, Artur**; **Tšertov, Anton**; **Ellervee, Peeter** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 55-58 : ill

Health management for self-aware SoCs based on IEEE 1687 infrastructure
Shibin, Konstantin; **Devadze, Sergei**; Jutman, Artur; Grabmann, Martin; Pricken, Robin IEEE Design & Test 2017 / p. 27-35 : ill https://doi.org/10.1109/MDAT.2017.2750902 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Hierarchical calculation of malicious faults for evaluating the fault-tolerance
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan**; **Jervan, Gert**; **Ellervee, Peeter** Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill https://ieeexplore.ieee.org/document/4459544

Hierarchical timing-critical paths analysis in sequential circuits
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan**; **Devadze, Sergei**; **Kostin, Sergei** 2018 IEEE 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS 2018) : 2 – 4 July 2018, Spain 2018 / 6 p. : ill https://doi.org/10.1109/PATMOS.2018.8464176

High-speed logic level fault simulation
Ubar, Raimund-Johannes; **Devadze, Sergei** Design and test technology for dependable systems-on-chip 2011 / p. 310-335 : ill
https://www.igi-global.com/chapter/high-speed-logic-level-fault/51407

HLS-based optimization of tau triggering algorithm for LHC: a case study

Cherezova, Natalia; **Mihhailov, Dmitri**; **Devadze, Sergei**; **Jutman, Artur** 2022 18th Biennial Baltic Electronics Conference (BEC) 2022 / 6 p. : ill https://doi.org/10.1109/BEC56180.2022.9935599

IEEE 1687 compliant ecosystem for embedded instrumentation access and in-field health monitoring
Tšertov, Anton; Jutman, Artur; Shibin, Konstantin; **Devadze, Sergei** IEEE AUTOTESTCON 2018 : National Harbor, September 17-20, 2018 : proceedings 2018 / 9 p.: ill https://doi.org/10.1109/AUTEST.2018.8532559

IEEE P1687 IJTAG demonstrator on FPGA
Shibin, Konstantin; **Aleksejev, Igor**; **Jutman, Artur**; **Devadze, Sergei** DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p. : ill
https://www.academia.edu/22101517/IEEE_P1687_IJTAG_demonstrator_on_FPGA

In-system programming of non-volatile memories on microprocessor-centric boards
Tšertov, Anton; **Devadze, Sergei**; **Jutman, Artur**; **Jasnetski, Artjom** International journal of microelectronics and computer science 2014 / p. 25-34 : ill

Invited paper: System-Wide Fault Management based on IEEE P1687 IJTAG
Jutman, Artur; **Devadze, Sergei**; **Aleksejev, Jevgeni** 6th International Workshop on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) : 20-22 June 2011, Montpeillier, France 2011 / [4] p.: ill https://ieeexplore.ieee.org/document/5981520

Java technology based training system for teaching digital design and test
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 283-286 : ill

Keynote: cost-efficient reliability for Edge-AI chips
Jenihhin, Maksim; **Taheri, Mahdi**; **Cherezova, Natalia**; **Ahmadilivani, Mohammad Hasan**; **Selg, Hardi**; **Jutman, Artur**; **Shibin, Konstantin**; **Tsertov, Anton**; **Devadze, Sergei**; **Kodamanchili, Rama Mounika**; **Rafiq, Ahsan**; **Raik, Jaan**; **Daneshtalab, Masoud** 2024 IEEE 25th Latin American Test Symposium (LATS) 2024 / 2 p https://doi.org/10.1109/LATS62223.2024.10534610 Article at Scopus

Learning digital test and diagnostics via internet
Ubar, Raimund-Johannes; **Jutman, Artur**; **Kruus, Margus**; **Orasson, Elmet**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International journal of online engineering 2007 / 1, [9] p. : ill https://www.db-thueringen.de/servlets/MCRFileNodeServlet/dbt_derivate_00032681/iJOE_1681-1221_03_2007_1_361.pdf

Learning digital test and diagnostics via internet [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Kruus, Margus**; **Orasson, Elmet**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International journal of computing & information sciences 2006 / 2, p. 86-96 : ill

Marginal PCB assembly defect detection on DDR3/4 memory bus
Odintsov, Sergei; **Jutman, Artur**; **Devadze, Sergei** 2017 IEEE International Test Conference (ITC 2017) : Forth Worth, Texas, USA, 31 October - 2 November 2017 2017 / p. 238-247 : ill https://doi.org/10.1109/TEST.2017.8242070 Conference proceedings at Scopus Article at Scopus Article at WOS

Microprocessor modeling for board level test access automation
Devadze, Sergei; **Jutman, Artur**; Tšertov, Anton; **Ubar, Raimund-Johannes** Proceedings of 10th IEEE Workshop on RTL and High Level Testing : Hong Kong, November 27-28, 2009 2009 / ? p

Microprocessor-based system test using debug interface
Devadze, Sergei; **Jutman, Artur**; **Tšertov, Anton**; Instenberg, Martin; **Ubar, Raimund-Johannes** 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 98-101 : ill http://dx.doi.org/10.1109/NORCHP.2008.4738291

On coverage of timing related faults at board level
Jutman, Artur; **Aleksejev, Igor**; **Devadze, Sergei** 2016 21st IEEE European Test Symposium (ETS) : May 23rd-26th 2016, Amsterdam, The Netherlands : proceedings 2016 / [2] p. : ill https://doi.org/10.1109/ETS.2016.7519295

On in-system programming of non-volatile memories
Tšertov, Anton; **Devadze, Sergei**; **Jutman, Artur**; **Jasnetski, Artjom** Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2013, Gdynia, Poland, June 20-22, 2013 2013 / p. 408-413 : ill

On in-system programming of non-volatile memories
Tšertov, Anton; **Devadze, Sergei**; **Jutman, Artur**; **Jasnetski, Artjom** International journal of microelectronics and computer science 2013 / p. 72-78 : ill

On-chip sensors data collection and analysis for SoC health management
Shibin, Konstantin; **Jenihhin, Maksim**; **Jutman, Artur**; Devadze, Sergei; Tsertov, Anton 2023 IEEE International Symposium on

Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2023 / 6 p https://doi.org/10.1109/DFT59622.2023.10313562

On-line fault classification and handling in IEEE1687 based fault management system for complex SoCs
Shibin, Konstantin; **Devadze, Sergei**; **Jutman, Artur** LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 69-74 : ill https://doi.org/10.1109/LATW.2016.7483342

Open-source JTAG simulator bundle for labs
Shibin, Konstantin; **Devadze, Sergei**; **Rosin, Vjatšeslav**; **Jutman, Artur**; **Ubar, Raimund-Johannes** International journal of electronics and telecommunications 2012 / p. 233-239 : ill https://journals.pan.pl/Content/87192/PDF/32.pdf

Optimization of boundary scan tests using FPGA-based efficient scan architectures
Aleksejev, Igor; **Devadze, Sergei**; **Jutman, Artur**; **Shibin, Konstantin** Journal of electronic testing : theory and applications (JETTA) 2016 / p. 245-255 : ill https://doi.org/10.1007/s10836-016-5588-y Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Parallel critical path tracing fault simulation in sequential circuits
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Kostin, Sergei**; **Devadze, Sergei**; **Raik, Jaan** Proceedings of 25th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS : MIXDES 2018 : Gdynia, Poland, June 21–23, 2018 2018 / p. 305-310 : ill https://doi.org/10.23919/MIXDES.2018.8436880

Parallel exact critical path tracing fault simulation with reduced memory requirements
Devadze, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Jutman, Artur** 4th International Conference on Design and Technology of Integrated Systems in Nanoscal Era : DTIS'09 : Cairo, Egypt, April 6-9, 2009 2009 / p. 155-160 : ill https://ieeexplore.ieee.org/document/4938046

Parallel fault analysis on structurally synthesized BDDs
Devadze, Sergei; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 47-50 : ill

Parallel fault backtracing for calculation of fault coverage
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** Proceedings of the ASP-DAC 2008 : [13th] Asia and South Pacific Design Automation Conference 2008 : January 21-24, 2008, COEX, Seoul, Korea 2008 / p. 667-672 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault backtracing for calculation of fault coverage
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 43rd International Conference on Microelectronics, Devices and Materials and the Workshop on Electronic Testing : September 12. - September 14.2007, Bled, Slovenia : MIDEM conference 2007 proceedings 2007 / p. 165-170 : ill https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel X-fault simulation with critical path tracing technique [Electronic resource]
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** DATE 10 : Design, Automation & Test in Europe : Dresden, Germany, 8-12 March, 2010 2010 / p. 879-884 [CD-ROM] https://www.researchgate.net/publication/221341788_Parallel_X-fault_simulation_with_critical_path_tracing_technique

Reliable health monitoring and fault management infrastructure based on embedded instrumentation and IEEE 1687
Jutman, Artur; **Shibin, Konstantin**; **Devadze, Sergei** IEEE AUTOTESTCON 2016 : Anaheim, California, USA, September 12-15, 2016 : proceedings 2016 / p. 240-249 : ill https://doi.org/10.1109/AUTEST.2016.7589605

Run-time reconfigurable instruments for advanced board-level testing
Aleksejev, Igor; **Jutman, Artur**; **Devadze, Sergei** IEEE AUTOTESTCON 2016 : Anaheim, California, USA, September 12-15, 2016 : proceedings 2016 / p. 385-392 : ill https://doi.org/10.1109/AUTEST.2016.7589627

Run-time reconfigurable instruments for advanced board-level testing
Aleksejev, Igor; **Jutman, Artur**; **Devadze, Sergei** IEEE instrumentation & measurement magazine 2017 / p. 23-30 : ill https://doi.org/10.1109/MIM.2017.8006390

SoC and board modeling for processor-centric board testing
Tšertov, Anton; **Ubar, Raimund-Johannes**; **Jutman, Artur**; **Devadze, Sergei** 14th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2011 : 31 August - 2 September 2011, Oulu, Finland : proceedings 2011 / p. 575-582 : ill https://ieeexplore.ieee.org/document/6037463

Software environment for synthesis of testable FSM through decomposition
Devadze, Sergei; **Sudnitsõn, Aleksander** 2008 26th International Conference on Microelectronics (MIEL 2008) : proceedings 2008 / p. 433-436 https://ieeexplore.ieee.org/document/4559314

Structurally synthesized multiple input BDDs for speeding up logic-level simulation of digital circuits

Mironov, Dmitri; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 13th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2010 : Lille, France, 1-3 September 2010 : proceedings 2010 / p. 658-663 : ill https://ieeexplore.ieee.org/document/5615526

A suite of IEEE 1687 benchmark networks
Tšertov, Anton; **Jutman, Artur**; **Devadze, Sergei** 2016 IEEE International Test Conference (ITC) : proceedings 2016 / art. 6.1, p. 1-10 : ill https://doi.org/10.1109/TEST.2016.7805840

Synchronization, calibration and triggering of IEEE 1687 embedded instruments
Jutman, Artur; **Devadze, Sergei**; **Shibin, Konstantin** The Seventeenth Workshop on RTL and High Level Testing (WRTLT'16) : November 24-25, 2016, Aki Grand Hotel, Hiroshima, Japan 2016 / [6] p

Synthesis of testable FSM through decomposition
Devadze, Sergei; **Sudnitsõn, Aleksander** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 101-104 : ill

System-wide fault management based on IEEE P1687 IJTAG
Shibin, Konstantin; **Jutman, Artur**; **Devadze, Sergei** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 81-84 : ill

Teaching digital RT-level self-test using a Java applet
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 322-328 : ill

Testing beyond the SoCs in a lego style
Tšertov, Anton; **Jutman, Artur**; **Devadze, Sergei** Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 334-338 : ill https://ieeexplore.ieee.org/document/5742052

Trainer 1149: a boundary scan simulation bundle for labs
Jutman, Artur; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; Shibin, Konstantin; Rosin, Vjatšeslav MIXDES 2011 : 18th International Conference "Mixed Design of Integrated Circuits and Systems" : June 16-18, 2011, Gliwice, Poland 2011 / p. 520-525

Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** Microprocessors and microsystems 2015 / p. 1130-1138 : ill https://doi.org/10.1016/j.micpro.2015.05.003 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Turning JTAG inside out for fast extended test access
Devadze, Sergei; **Jutman, Artur**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes** 10th IEEE Latin American Test Workshop : 2-5 March 2009, Brazil 2009 / [6] p. : ill https://ieeexplore.ieee.org/document/4813799

Ultra fast parallel fault analysis on structurally synthesized BDDs
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 131-136 : ill http://dx.doi.org/10.1109/ETS.2007.43

Understanding boundary scan test with Trainer 1149
Jutman, Artur; **Devadze, Sergei**; **Shibin, Konstantin**; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** 22nd EAEEIE annual conference : June, 13-15, 2011, Maribor, Slovenija : conference book 2011 / p. 21-22 https://ieeexplore.ieee.org/document/6165727

Ways for board and system test to benefit from FPGA embedded instrumentation
Ehrenberg, Heiko; **Odintsov, Sergei**; **Devadze, Sergei**; **Jutman, Artur**; **Aleksejev, Igor**; Wenzel, Thomas 2019 IEEE AUTOTESTCON 2019 / 10 p : ill https://doi.org/10.1109/AUTOTESTCON43700.2019.8961057

Web based tools for synthesis and testing of digital devices
Devadze, Sergei; **Jutman, Artur**; **Kruus, Margus**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** Proceedings of the International Conference on Computer Systems and Technologies (e-Learning) : CompSysTech'2002, Sofia, Bulgaria, 20-21 June 2002 / p. 1.9-1 - 1.9-6 : ill
https://www.researchgate.net/publication/250738271_Web_Based_Tools_for_Synthesis_and_Testing_of_Digital_Devices

Web-based computer aided design support of finite state machine additive decomposition for low power
Sudnitsõn, Aleksander; **Devadze, Sergei** 5th IEEE East-West Design & Test International Symposium 2007 / p. 494-498

Web-based software implementation of finite state machine decomposition for design and education
Devadze, Sergei; **Kruus, Margus**; **Sudnitsõn, Aleksander** CompSysTech' 2001 : proceedings of the International Conference on Computer Systems and Technologies, Sofia, 21-22 June 2001 2001 / [6] p. : ill
https://pld.ttu.ee/decomposition/publications/Sudnitson_CST_Estonia.pdf

Web-based system for sequential machines decomposition
Devadze, Sergei; **Fomina, Jelena**; **Kruus, Margus**; **Sudnitsõn, Aleksander** The IEEE Region 8 EUROCON 2003 : Computer as a Tool : 22-24. September 2003, Ljubljana, Slovenia : proceedings. Volume A 2003 / p. 57-61 : ill
https://pld.ttu.ee/decomposition/publications/Sudnitson-EUROCON_v5%20_1_.pdf

Web-based training system for teaching basics of RT-level digital design, test, and design for test [Electronic resource]
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [6] p. : ill. [CD-ROM]

Web-based training system for teaching digital design and test
Devadze, Sergei 7th International Student Conference on Electrical Engineering : POSTER2003 : May 22, 2003, Prague, Czech Republic 2003 / p. IC6

Virtual reconfigurable scan-chains on FPGAs for optimized board test
Aleksejev, Igor; **Jutman, Artur**; **Devadze, Sergei**; **Shibin, Konstantin** 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill http://dx.doi.org/10.1109/LATW.2015.7102411