

Automated design error debug using high-level decision diagrams and mutation operators

Raik, Jaan; Repinski, Urmaz; Tšepurov, Anton; Hantson, Hanno; Ubar, Raimund-Johannes; Jenihhin, Maksim

Microprocessors and microsystems 2013 / p. 505-513 : ill

An automated method for mining high-quality assertion sets

Heidari Iman, Mohammadreza; Raik, Jaan; Jenihhin, Maksim; Jervan, Gert; Ghasempouri, Tara Microprocessors and

microsystems 2023 / art. 104773 <https://doi.org/10.1016/j.micpro.2023.104773>

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art.

103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Design and verification of Cyber-Physical Systems using TrueTime, evolutionary optimization and UPPAAL

Balasubramanian, Sreeram; Srinivasan, Seshadhri; Buonopane, Furio; Balasubramanian, Subathra; Vain, Jüri; Ramaswamy, Srin

Microprocessors and microsystems 2016 / p. 37-48 : ill <http://dx.doi.org/10.1016/j.micpro.2015.12.006>

Design of Cyber Bio-analytical Physical Systems : formal methods, architectures, and multi-system interaction strategies

Ashraf, Kanwal; Le Moullec, Yannick; Pardy, Tamas; Rang, Toomas Microprocessors and microsystems 2023 / art. 104780, 14

p. : ill <https://doi.org/10.1016/j.micpro.2023.104780>

Embedded fault diagnosis in digital systems with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan Microprocessors and microsystems 2008 / 5/6, p. 279-287 : ill

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and

microsystems 2015 / p. 909-918 : ill <http://dx.doi.org/10.1016/j.micpro.2014.11.002>

Guest editorial

Ellervee, Peeter; Nurmi, Jari Microprocessors and microsystems 2013 / p. 430-431

Hybrid BIST optimization using reseeding and test set compaction

Jervan, Gert; Orasson, Elmet; Kruus, Helena; Ubar, Raimund-Johannes Microprocessors and microsystems 2008 / 5/6, p. 254-

262 : ill

Modeling and simulation of circuits with shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan; Viies, Vladimir Microprocessors and microsystems 2017 / p. 56-61 : ill

<http://dx.doi.org/10.1016/j.micpro.2016.09.006>

Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan Microprocessors and microsystems 2015 / p. 1130-

1138 : ill <http://dx.doi.org/10.1016/j.micpro.2015.05.003>

Understanding multidimensional verification : where functional meets non-functional

Lai, Xinhui; Balakrishnan, Aneesh; Lange, Thomas; Jenihhin, Maksim; Ghasempouri, Tara; Raik, Jaan; Alexandrescu, Dan

Microprocessors and microsystems 2019 / art. 102867, 13 p. : ill <https://doi.org/10.1016/j.micpro.2019.102867> [Journal metrics at Scopus](#)

[Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)