

An approach for verification assertions reuse in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Viilukas, Taavi Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTL'T'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

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Constraint-based hierarchical untestability identification for synchronous sequential circuits

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Identifying untestable faults in sequential circuits using test path constraints

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RT-level identification of potentially testable initialization faults

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Untestable fault identification in sequential circuits using model-checking

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