Automated design error debug using high-level decision diagrams and mutation operators
Raik, Jaan; **Repinski, Urmas**; **Tšepurov, Anton**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**
Microprocessors and microsystems 2013 / p. 505-513 : ill

Combining dynamic slicing and mutation operators for ESL correction
Repinski, Urmas; **Hantson, Hanno**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / [6] p. : ill

Comparison of model-based error localization algorithms for C designs
Repinski, Urmas; **Raik, Jaan** Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 42-45

Design error diagnosis using backtrace algorithm on decision diagrams
Repinski, Urmas; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis
Hantson, Hanno; **Repinski, Urmas**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes** LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill

FoREnSiC– an automatic debugging environment for C programs
Bloem, Roderick; **Raik, Jaan**; **Repinski, Urmas** Eighth Haifa Verification Conference : HVC 2012 : November 6-8, Haifa, Israel : [proceedings] 2012 / p. 1-6 : ill

High-level decision diagram simulation for diagnosis and soft-error analysis
Raik, Jaan; **Repinski, Urmas**; **Jenihhin, Maksim**; **Chepurov, Anton** Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill

High-level design error diagnosis using backtrace on decision diagrams
Raik, Jaan; **Repinski, Urmas**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill
http://dx.doi.org/10.1109/NORCHIP.2010.5669486

Model-based verification with error localization and error correction for C designs
Repinski, Urmas Программные продукты и системы = Programmnye produkty i sistemy = Software & systems 2012 / p. 221-229 : ill

Верификация на основе симуляции с нахождением и исправлением ошибок для С-дизайнов
Repinski, Urmas Программные продукты и системы = Programmnye produkty i sistemy = Software & systems 2012 / с. 229-237 : ил