

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill

On the reuse of TLM mutation analysis at RTL

Guarnieri, Valerio; **Hantson, Hanno; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2012 / p. 435-448 : ill