

A scalable model based RTL framework zamiaCAD for static analysis

Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Tihhomirov, Valentin 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill <https://www.semanticscholar.org/paper/A-scalable-model-based-RTL-framework-zamiaCAD-for-Tšepurov-Bartsch/d19eefa44f793621d537c06498784e06e0332fd2>

Applications of the open source HW design framework zamiaCAD

Tšepurov, Anton; Tihhomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

Assessment of diagnostic test for automated bug localization

Tihhomirov, Valentin; Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

Automated design error localization in RTL designs

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Diagnostic test generation for statistical bug localization using evolutionary computation

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Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

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Localization of bugs in processor designs using zamiaCAD framework

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Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG

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Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs

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zamiaCAD : understand, develop and debug hardware designs

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Using simulation statistics for bug localization in RTL designs

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VHDL design debug framework based on zamiaCAD

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