

## A scalable model based RTL framework zamiaCAD for static analysis

**Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Tihhomirov, Valentin** 2012 IEEE/IFIP 20th International Conference on VLSI and System-on-Chip (VLSI-SoC) : October 7-10, 2012 Santa Cruz, USA Dream Inn, Santa Cruz, USA : [proceedings] 2012 / p. 171-176 : ill

## Applications of the open source HW design framework zamiaCAD

**Tšepurov, Anton; Tihhomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan** DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

## Assessment of diagnostic test for automated bug localization

**Tihhomirov, Valentin; Tšepurov, Anton; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes** LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

## Automated design error localization in RTL designs

**Jenihhin, Maksim; Tšepurov, Anton; Tihhomirov, Valentin; Raik, Jaan; Hantson, Hanno; Ubar, Raimund-Johannes; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich** IEEE design & test of computers 2014 / p. 83-92 : ill  
<http://dx.doi.org/10.1109/MDAT.2013.2271420>

## Diagnostic test generation for statistical bug localization using evolutionary computation

**Gaudesi, Marco; Jenihhin, Maksim; Raik, Jaan; Tihhomirov, Valentin; Ubar, Raimund-Johannes** Applications of Evolutionary Computation : 17th European Conference, EvoApplications 2014, Granada, Spain, April 23-25, 2014 : revised selected papers 2014 / p. 425-436 : ill

## Environment for fault simulation acceleration on FPGA

**Ellervee, Peeter; Raik, Jaan; Tihhomirov, Valentin** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 217-220 : ill

## Evaluating fault emulation on FPGA

**Ellervee, Peeter; Raik, Jaan; Tihhomirov, Valentin; Tammeäe, Kalle** Field-Programmable Logic and Applications : 14th International Conference, FPL 2004 : Antwerp, Belgium, August 30-September 1, 2004 : proceedings 2004 / p. 354-363 : ill

## Fast fault emulation for synchronous sequential circuits

**Raik, Jaan; Ellervee, Peeter; Tihhomirov, Valentin; Ubar, Raimund-Johannes** Proceedings of East-West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 35-40  
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## Fault emulation on FPGA : a feasibility study

**Ellervee, Peeter; Raik, Jaan; Tihhomirov, Valentin** IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 92-95 : ill

## FPGA based fault emulation of synchronous sequential circuits

**Ellervee, Peeter; Raik, Jaan; Tihhomirov, Valentin; Ubar, Raimund-Johannes** Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 59-62 <https://ieeexplore.ieee.org/abstract/document/1423822>

## Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

**Jenihhin, Maksim; Squillero, Giovanni; Tihhomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <http://dx.doi.org/10.1007/s10836-016-5589-x>

## Improved fault emulation for synchronous sequential circuits

**Raik, Jaan; Ellervee, Peeter; Tihhomirov, Valentin; Ubar, Raimund-Johannes** Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

## Localization of bugs in processor designs using zamiaCAD framework

**Tšepurov, Anton; Tihhomirov, Valentin; Jenihhin, Maksim; Raik, Jaan** 13th International Workshop on Microprocessor Test and Verification (MTV 2012) Common Challenges and Solutions : Austin, USA, December 10-12, 2012 2012 / p. 1-6

## PSL assertion checkers synthesis with ASM based HLS tool ABELITE

**Jenihhin, Maksim; Baranov, Samary; Raik, Jaan; Tihhomirov, Valentin** LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill <https://ieeexplore.ieee.org/document/6261251>

## Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG

**Palermo, N.; Tihhomirov, Valentin; Copetti, Thiago; Jenihhin, Maksim; Raik, Jaan; Kostin, Sergei** 2015 16th Latin American Test Symposium (LATST 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill  
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**Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs**

Pellerey, Francesco; **Jenihhin, Maksim**; Squillero, Giovanni; **Raik, Jaan**; Sonza Reorda, Matteo; **Tihhomirov, Valentin**; Ubar, Raimund-Johannes 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill  
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**zamiaCAD : understand, develop and debug hardware designs**

**Jenihhin, Maksim**; **Tihhomirov, Valentin**; **Saif Abrar, Syed**; **Raik, Jaan**; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

**Using simulation statistics for bug localization in RTL designs**

**Tihhomirov, Valentin**; **Jenihhin, Maksim**; **Raik, Jaan** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 107-110 : ill

**VHDL design debug framework based on zamiaCAD**

**Tihhomirov, Valentin**; **Tsepurov, Anton**; **Saif Abrar, Syed**; **Jenihhin, Maksim**; **Raik, Jaan** DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill