

An approach to system-level design for test

Jervan, Gert; Ubar, Raimund-Johannes; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 121-149 : ill

Digital design flow with test activities

Diener, Karl-Heinz; Elst, G.; **Ivask, Eero; Jervan, Gert;** Peng, Z.; **Raik, Jaan; Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

High-level synthesis and test in the MOSCITO-based virtual laboratory

Schneider, Andre; Diener, Karl-Heinz; **Jervan, Gert;** Peng, Z.; **Raik, Jaan; Ubar, Raimund-Johannes;** Hollstein, Thomas; Glesner, M. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 287-290 : ill

Improving the efficiency of timing simulation in digital circuits by using structurally synthesized BDDs

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. IEEE Norchip Conference 2000 / p. 254-261

An iterative approach to test time minimization for parallel hybrid BIST architecture

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Z. 5th IEEE Latin-American Test Workshop - LATW 2004 : Cartagena, Colombia, 2004 : digest of papers 2004 / p. 98-103 : ill <https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf>

An iterative approach to test time minimization for parallel hybrid BIST architectures

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Z. System-on-Chip Conference 2004 : Bastad, Sweden 2004 / p. ? <https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf>

Test generation : a hierarchical approach

Jervan, Gert; Ubar, Raimund-Johannes; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 67-81 : ill

Test generation for digital systems at functional level

Ubar, Raimund-Johannes; Kuchcinski, Ktysztof; Peng, Z. Research report LiTH-IDA-R-90-06, Linköping University, Sweden 1990 / p. 1-21

Timing simulation of digital circuits with binary decision diagrams

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill <https://ieeexplore.ieee.org/document/915063>

Using Tabu search method for optimizing the cost of hybrid BIST

Kruus, Helena; **Ubar, Raimund-Johannes; Jervan, Gert;** Peng, Z. XVI Conference on Design of Circuits and Integrated Systems : Porto, Portugal, 2001 2001 / p. 445-450 <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e97bb394ff71aa0affcc5fb372404bbc246888a8>

Virtual laboratory for research in dependable microelectronics

Diener, Karl-Heinz; Elst, G.; Gramatova, Elena; Kuzmich, W.; Peng, Z.; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 217-220 : ill