

**Checking sequence design for FSM**

**Keevallik, Andres; Kruus, Margus; Lensen, Harri** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 325-330

**Mixed-level deterministic-random test generation for digital systems**

**Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 335-340

**Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation**

Leveugle, R.; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358