

## **Power-performance trade-offs in second level memory used by an ARM-like Risc architecture**

Puttaswamy, Kiran; **Ellervee, Peeter** Power aware computing 2002 / ? p. [chapter 11] [https://link.springer.com/chapter/10.1007/978-1-4757-6217-4\\_11](https://link.springer.com/chapter/10.1007/978-1-4757-6217-4_11)