

### **Comparative analysis of sequential circuit test generation approaches**

**Raik, Jaan; Krivenko, Anna; Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 225-228 : ill

### **Constraint-based test pattern generation at the register-transfer level**

**Viilukas, Taavi; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Krivenko, Anna** Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14-16, 2010, Vienna, Austria 2010 / p. 352-357 : ill  
<http://dx.doi.org/10.1109/DDECS.2010.5491752>

### **Hierarchical identification of untestable faults in sequential circuits**

**Raik, Jaan; Ubar, Raimund-Johannes; Krivenko, Anna; Kruus, Margus** 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 668-671 : ill  
<http://dx.doi.org/10.1109/DSD.2007.4341539>

### **New technique for hierarchical identification of untestable faults in sequential circuits**

**Krivenko, Anna; Ubar, Raimund-Johannes; Raik, Jaan; Kruus, Margus** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / lk. 155-158 : ill

### **RT-level identification of potentially testable initialization faults**

**Raik, Jaan; Fujiwara, Hideo; Krivenko, Anna** The Ninth IEEE Workshop on RTL and High Level Testing (WRTL 2008), Sapporo, Japan 2008 / [6] p [https://www.researchgate.net/publication/234032548\\_RT-level\\_identification\\_of\\_potentially\\_testable\\_initialization\\_faults](https://www.researchgate.net/publication/234032548_RT-level_identification_of_potentially_testable_initialization_faults)

### **Untestable fault identification in sequential circuits using model-checking**

**Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Krivenko, Anna** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 257-262 : ill <https://ieeexplore.ieee.org/document/4711554>

### **Untestable fault identification in sequential circuits using model-checking**

**Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Krivenko, Anna** Proceedings of the 17th Asian Test Symposium ATS 2008 : November 24-27, 2008, Sapporo, Japan 2008 / p. 21-26 : ill <http://dx.doi.org/10.1109/ATS.2008.22>