

Defect-oriented test- and layout-generation for standard-cell ASIC designs

Sudbrock, Joachim; **Raik, Jaan; Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill <https://ieeexplore.ieee.org/document/1559781>

Deterministic defect-oriented test generation for combinational circuits

Raik, Jaan; Ubar, Raimund-Johannes; Sudbrock, Joachim; Kuzmicz, Wieslaw; Pleskacz, Witold A. LATW 2005 : 6th IEEE Latin-American Test Workshop : March 30 - April 2, 2005, Salvador, Bahia, Brazil : [digest of papers] 2005 / p. 325-330 : ill

DOT: new deterministic defect-oriented ATPG tool

Raik, Jaan; Ubar, Raimund-Johannes; Sudbrock, Joachim; Kuzmicz, Wieslaw; Pleskacz, Witold A. European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings 2005 / p. 96-101 : ill