

Automatic SoC level test path synthesis based on partial functional models

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 <https://ieeexplore.ieee.org/document/6114730>

Decision diagrams - from a mathematical notion to engineering applications

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How to generate high quality tests for digital systems

Ubar, Raimund-Johannes; Aarna, Margit; Kruus, Helena; Raik, Jaan 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill <http://dx.doi.org/10.1109/SMICND.2004.1403048>