

Abstraction of clock interface for conversion of RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Applications of the open source HW design framework zamiaCAD

Tšepurov, Anton; Tihhomirov, Valentin; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2012 University Booth : Design Automation and Test in Europe : Dresden, Germany, March 12-16, 2012 2012 / 1 p

Extensible open-source framework for translating RTL VHDL IP cores to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

Open-source framework and practical considerations for translating RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2012 : IP Embedded System Conference & Exhibition : Grenoble, France, Dec. 4-5, 2012 2012 <https://www.design-reuse.com/articles/32685/translating-rtl-vhdl-to-systemc.html>

Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan IP-SoC 2013 : IP embedded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

Performance analysis of cosimulating processor core in VHDL and SystemC

Saif Abrar, Syed; Shyam Kiran A.; Jenihhin, Maksim; Raik, Jaan; Babu, C. Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22–25 August 2013, Mysore, India 2013 / p. 563-568 : ill

zamiaCAD : understand, develop and debug hardware designs

Jenihhin, Maksim; Tihhomirov, Valentin; Saif Abrar, Syed; Raik, Jaan; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

VHDL design debug framework based on zamiaCAD

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