

Analysis and comparison of attainable hardware acceleration in all programmable systems-on-chip

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At-speed testing of inter-die connections of 3D-SICs in the presence of shore logic

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DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

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A framework for comprehensive automated evaluation of concurrent online checkers

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How to prove that a circuit is fault-free?

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Identifying NBTI-critical paths in nanoscale logic

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