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Wafer-level die re-test success prediction using machine learning

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<https://doi.org/10.1109/LATS49555.2020.9093672>

VHDL design debug framework based on zamiaCAD

Tihhomirov, Valentin; Tšepurov, Anton; Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill