

A synthesis-agnostic behavioral fault model for high gate-level fault coverage

Karputkin, Anton; Raik, Jaan Proceedings of the 2016 Design, Automation & Test in Europe Conference & Exhibition (DATE) : 14-18 March 2016, ICC, Dresden, Germany 2016 / p. 1124-1127 : ill <https://ieeexplore.ieee.org/document/7459477/figures#figures>

Automated correction of design errors by edge redirection on high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Tombak, Mati; Raik, Jaan 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill <https://ieeexplore.ieee.org/document/6113980>

Canonical representations of high-level decision diagrams

Karputkin, Anton; Ubar, Raimund-Johannes; Raik, Jaan; Tombak, Mati Estonian journal of engineering 2010 / 1, p. 39-55 : ill

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel

Karputkin, Anton 2012

Generating directed tests for C programs using RTL ATPG

Raik, Jaan; Drenkhan, Tiia; Jenihhin, Maksim; Viilukas, Taavi; Karputkin, Anton; Tšepurov, Anton; Ubar, Raimund-Johannes Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTL'12) 2012 / p. 1-6

High level decision diagrams and characteristic polynomials

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Probabilistic equivalence checking based on high-level decision diagrams

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Synthesis of high-level decision diagrams for functional test pattern generation

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Verification and error correction on High-Level Decision Diagrams

Karputkin, Anton 2013