Abstraction of clock interface for conversion of RTL VHDL to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Comprehensive abstraction of VHDL RTL cores to ESL SystemC = Register-siirde taseme VHDL kirjelduste kompleksne abstraheerimine süsteemitaseme SystemC mudeliteks
Abrar, Syed Saif 2016 http://www.ester.ee/record=b4564850*est

Extensible open-source framework for translating RTL VHDL IP cores to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

FSMD RTL design manipulation for clock interface abstraction
Abrar, Syed Saif; **Jenihhin, Maksim**; **Raik, Jaan** 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 10-13 August 2015, Kerala, India 2015 / p. 463-468 : ill http://dx.doi.org/10.1109/ICACCI.2015.7275652

Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** IP-SoC 2013 : IP embbeded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

Performance analysis of cosimulating processor core in VHDL and SystemC
Saif Abrar, Syed; Shyam Kiran A.; **Jenihhin, Maksim**; **Raik, Jaan**; Babu, C. Proceedings of the 2013 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 22–25 August 2013, Mysore, India 2013 / p. 563-568 : ill

SystemC-based loose models : RTL abstraction for design understanding
Abrar, Syed Saif; **Jenihhin, Maksim**; **Raik, Jaan** Workshop on Design Automation for Understanding Hardware Designs DUHDe 2015 : Grenoble, March 13, 2015 2015 / p. 1-6

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores
Abrar, Syed Saif; **Jenihhin, Maksim**; **Raik, Jaan** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill
http://dx.doi.org/10.1109/DDECS.2015.39