

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

Combinational fault simulation in sequential circuits

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Comparison of two approaches to improve functional BIST fault coverage

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Environment for the analysis of functional self-test quality in digital systems

Ubar, Raimund-Johannes; Kostin, Sergei; Kruus, Helena; Aarna, Margit; Devadze, Sergei Proceedings of the Estonian Academy of Sciences 2014 / p. 151-162 : ill https://artiklid.elnet.ee/record=b2673964*est

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <http://dx.doi.org/10.1016/j.micpro.2014.11.002>

Parallel critical path tracing fault simulation in sequential circuits

Kõusaar, Jaak; Ubar, Raimund-Johannes; Kostin, Sergei; Devadze, Sergei; Raik, Jaan Proceedings of 25th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS : MIXDES 2018 : Gdynia, Poland, June 21–23, 2018 2018 / p. 305-310 : ill <https://doi.org/10.23919/MIXDES.2018.8436880>

Self-testing of pipe-lined signal processing architectures at-speed

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