

A scalable technique to identify true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan Proceedings 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit & Systems (DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 152-157 : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553>

A tool set for teaching design-for-testability of digital circuits

Kostin, Sergei; Orasson, Elmet; Ubar, Raimund-Johannes EWME 2016 : 11th European Workshop on Microelectronics Education : May 11-13, 2016, Southampton, UK 2016 / [6] p. : ill <http://dx.doi.org/10.1109/EWME.2016.7496466>

Boole'i algebra kasutamine automaatikalülituste projekteerimisel : loengukonspekt

Agur, Ustus 1972 https://www.ester.ee/record=b1327567*est

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Combinational fault simulation in sequential circuits

Ubar, Raimund-Johannes; Kõusaar, Jaak; Gorev, Maksim; Devadze, Sergei 2015 IEEE International Symposium on Circuits and Systems : 24-27 May 2015, Lisboa, Portugal : [proceedings] 2015 / p. 2876-2879 : ill

Complex delay fault reasoning with sequential 7-valued algebra

Kõusaar, Jaak; Ubar, Raimund-Johannes; Alekseev, Igor 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill <http://dx.doi.org/10.1109/LATW.2015.7102403>

Computational aspects of nodal method for simulation of electronic circuits

Laksberg, Edgar 1983

Computer-aided examination of the P^L current source and the behaviour of the P^L flip-flop used in static memory cells

Rang, Toomas Periodica polytechnica. Electrical engineering = Электротехника 1981 / p. 159-165 : joon https://www.ester.ee/record=b1198855*est <https://pp.bme.hu/ee/article/view/4776/3881>

Conditional fault collapsing in digital circuits with shared structurally synthesized BDDs [Online resource]

Jürimägi, Lembit; Ubar, Raimund-Johannes BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p. : ill <https://doi.org/10.1109/BEC.2018.8600967>

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 61-66 : ill

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 108-113 : ill

Defects, faults and fault models

Gramatova, Elena; Fisherova, Maria; **Ubar, Raimund-Johannes**; Pleskacz, Witold A. Handbook of testing electronic systems 2005 / p. 26-96 : ill

Design error diagnosis in digital circuits with stuck-at fault model

Jutman, Artur; Ubar, Raimund-Johannes Microelectronics reliability 2000 / 2, p. 307-320 : ill

Diagnostics system for electronic circuits

Melentjev, Sergei 11th International Symposium "Topical Problems in the Field of Electrical and Power Engineering." Doctoral School of Energy and Geotechnology II : Pärnu, Estonia, January 16-21, 2012 2012 / p. 192-194 : ill

Digitaalsüsteemide diagnostika

Ubar, Raimund-Johannes 2005 http://www.ester.ee/record=b2097071*est

Ein universeller Weg zur Automatisierung des Testentwurfs für digitale Objecte

Ubar, Raimund-Johannes; Lohuaru, Tõnu Fehler in Automaten 1989 / S. 16-30 : ill

Electronic circuits : examples for project based subject "Technologies of electronic products"

Sillakivi, Peeter; Tamm, Uljas 2003 https://www.ester.ee/record=b1828290*est

Elektronilülitused : näidisskeemid projektipõhilisele õppeainele "Elektrontoodete tehnoloogiad"

2003 https://www.ester.ee/record=b1828299*est

European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings

Cantarella, JD 2005 https://www.ester.ee/record=b2300865*est

Evolutionary approach to test generation for functional BIST

Skobtsov, Y.A.; Ivanov, D.E.; Skobtsov, V.Y.; **Ubar, Raimund-Johannes; Raik, Jaan** Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. 151-155 : ill https://artiklid.elnet.ee/record=b1018764*est

Exact parallel critical path fault tracing to speed-up fault simulation in sequential circuits

Kõusaar, Jaak; Ubar, Raimund-Johannes; Kostin, Sergei; Devadze, Sergei; Raik, Jaan International journal of microelectronics and computer science 2018 / p. 9-18 <https://ijmcs.dmcps.pl/web/guest/vol.-9-no.-1>
https://ijmcs.dmcps.pl/documents/10630/345460/IJMCS_1_2018_2.pdf

Fast identification of true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan; Jürimägi, Lembit Microelectronics reliability 2018 / p. 252-261 : ill <https://doi.org/10.1016/j.microrel.2017.11.027> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fault simulation with parallel exact critical path tracing in multiple core environment

Gorev, Maksim; Ubar, Raimund-Johannes; Devadze, Sergei Proceedings of the 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE) : 9-13 March 2015, Grenoble, France 2015 / p. 1180-1185 : ill

Handbook of testing electronic systems

Novak, Ondrej; Gramatova, Elena; **Ubar, Raimund-Johannes; Jutman, Artur; Raik, Jaan** 2005
https://www.ester.ee/record=b2102523*est

Hierarchical identification of NBTI-critical gates in nanoscale logic

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Hierarchical identification of untestable faults in sequential circuits

Raik, Jaan; Ubar, Raimund-Johannes; Krivenko, Anna; Kruus, Margus 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 668-671 : ill
<http://dx.doi.org/10.1109/DSD.2007.4341539>

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits

Jenihhin, Maksim; Squillero, Giovanni; Tihomirov, Valentin; Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill <http://dx.doi.org/10.1007/s10836-016-5589-x>

Identification and rejuvenation of NBTI-critical paths in nanoscale logic circuits

Jenihhin, Maksim 1st International Workshop on Reliability and Aging in Forthcoming Electronic Systems : May 28-29, 2015, Cluj-Napoca, Romania 2015 / [1] p

Impulss-seadmed : laboratoorne töö nr. 5 : trigerid loogikaelementidel

1986 https://www.ester.ee/record=b1240931*est

Impulss-seadmed : laboratoorne töö nr. 8 : lineaarpinge generaator

1986 https://www.ester.ee/record=b2618544*est

Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005

2005 https://www.ester.ee/record=b2055139*est

Investigating defects in digital circuits by Boolean differential equations

Kruus, Helena; Orasson, Elmet; Robal, Tarmo; Ubar, Raimund-Johannes The 4th International Conference "Distance Learning - Educational Sphere of XXI Century" (DLESC'04) 2004 / p. 432-435

Low frequency acoustic method to measure the complex bulk modulus of porous materials

Napolitano, Marialuisa; Di Giulio, Elio; **Auriemma, Fabio** The Journal of the Acoustical Society of America 2022 / art. 1545
<https://doi.org/10.1121/10.0009767> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Modeling and simulation of circuits with shared structurally synthesized BDDs

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan; Viies, Vladimir Microprocessors and microsystems 2017 / p. 56-61 : ill
<http://dx.doi.org/10.1016/j.micpro.2016.09.006>

Multiple control fault testing in digital systems with high-level decision diagrams

Ubar, Raimund-Johannes; Oyeniran, Adeboye Stephen 2016 IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR) : THETA 20th edition : 19th-21st May, Cluj-Napoca, Romania : proceedings 2016 / [6] p. : ill
<http://dx.doi.org/10.1109/AQTR.2016.7501287>

Multiple fault analyses in logic circuits

Ubar, Raimund-Johannes IFAC-Symposium Discrete Systems : Dresden, 14.-19. 3. 77 1977 / p. [?]

Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia

2012 http://www.ester.ee/record=b2777270*est

Product and manufacturing in electronics : supplementary material in the subject "Technologies of electronic circuits"

Rang, Toomas 2003 https://www.ester.ee/record=b1766953*est

Rejuvenation of nanoscale logic at NBTI-critical paths using evolutionary TPG

Palermo, N.; **Tihomirov, Valentin**; Copetti, Thiago; **Jenihhin, Maksim**; **Raik, Jaan**; **Kostin, Sergei** 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill
<http://dx.doi.org/10.1109/LATW.2015.7102405>

Scalable algorithm for structural fault collapsing in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Orasson, Elmet; Raik, Jaan 2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 5-7, 2015, Daejeon, Korea 2015 / p. 171-176 : ill

7-valued algebra for transition delay fault analysis

Kõusaar, Jaak; Ubar, Raimund-Johannes BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 89-92 : ill

Shared Structurally Synthesized BDDs for speeding-up parallel pattern simulation in digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Raik, Jaan 2015 Nordic Circuits and Systems Conference (NORCAS) : NORCHIP & International Symposium on System-on-Chip (SoC) : 1st IEEE NORCAS Conference : 26-28 October 2015, Oslo, Norway 2015 / [4] p. : ill <http://dx.doi.org/10.1109/NORCHIP.2015.7364406>

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic

Kostin, Sergei; Raik, Jaan; Ubar, Raimund-Johannes; Jenihhin, Maksim 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

State of charge estimation for Li-ion batteries based on equivalent circuit diagrams and the application of a Kalman filter

Rahmoun, Ahmad; Biechl, Helmuth; **Rosin, Argo** 12th International Symposium "Topical Problems in the Field of Electrical and Power Engineering." Doctoral School of Energy and Geotechnology II : Kuressaare, Estonia, June 11-16, 2012 2012 / p. 125-128 : ill

Symbolic test generation for hierarchically modeled digital systems

Zaugarov, Viktor 1993 https://www.ester.ee/record=b2090336*est

10th IEEE European Test Symposium

Ubar, Raimund-Johannes; Prinetto, Paolo; Raik, Jaan IEEE journal of design & test of computers 2005 / p. 480-481 : phot
<http://dx.doi.org/10.1109/MDT.2005.106>

Testing tools

Jutman, Artur Handbook of testing electronic systems 2005 / p. 361-365 : ill

Testing tools

Raik, Jaan Handbook of testing electronic systems 2005 / p. 373-378 : ill

Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan Microprocessors and microsystems 2015 / p. 1130-1138 : ill <http://dx.doi.org/10.1016/j.micpro.2015.05.003>

Ökonoomsete negatiivse diferentsiaaltakistusega astmete ja elementide disainimine ja optimeerimine

Taniloo, Rainer 2005 https://www.ester.ee/record=b2073482*est

Генерирование тестов для цифровых схем при помощи модели альтернативных графов

Ubar, Raimund-Johannes Труды по электротехнике и автоматике. 14 1976 / с. 75-81 https://www.ester.ee/record=b2190768*est
<https://digikogu.taltech.ee/et/Item/aa35e320-87b1-405b-9cac-3b90c51867d1>

Диалоговая система моделирования электронных схем "ПОИСК"

Laksberg, Edgar; Nelus, K.; Ess, Viktor Методы и устройства регистрации, передачи, обработки и представления информации 1986 / с. 63-68

Единый подход к синтезу тестов цифровых схем и систем

Ubar, Raimund-Johannes Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 75-81 : илл https://www.ester.ee/record=b1237891*est

Импульсные устройства : лабораторная работа No 5 : триггеры на логических элементах

1988 https://www.ester.ee/record=b1224918*est

Исследование алгоритмов преобразования и аппроксимации параметров линейных систем и цепей на ЭВМ : автореферат ... кандидата технических наук (05.13.01)

Rüstern, Ennu 1976 https://www.ester.ee/record=b1301697*est

Исследование алгоритмов преобразования и аппроксимации параметров линейных систем и цепей на ЭВМ : диссертация на соискание ученой степени кандидата технических наук

Rüstern, Ennu 1975 https://www.ester.ee/record=b4630872*est

О выборе варьируемых элементов при оптимизации электронных схем

Laksberg, Edgar; Ess, Viktor Труды по радиотехнике. 3 1976 / с. 3-8 : илл https://www.ester.ee/record=b2190765*est
<https://digikogu.taltech.ee/et/Item/051089c8-3240-47a7-84ae-2e65ba92e5fb>

Об общей постановке задач тестовой диагностики цифровых схем

Ubar, Raimund-Johannes Труды по электротехнике и автоматике. 14 1976 / с. 69-73 https://www.ester.ee/record=b2190768*est
<https://digikogu.taltech.ee/et/Item/aa35e320-87b1-405b-9cac-3b90c51867d1>

Организация тестовых экспериментов цифровых систем на основе модели альтернативных графов

Lohuuri, Tõnu Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 47-52 https://www.ester.ee/record=b1237891*est

Применение алгебры Буля при проектировании схем автоматики : конспект лекций

Agur, Ustus 1974 https://www.ester.ee/record=b1292481*est

Руководство по применению пакета прикладных программ анализа и оптимизации электронных схем "ПОИСК"

1983 https://www.ester.ee/record=b1271968*est

Тестовая диагностика цифровых устройств : учебное пособие. II, Синтез и анализ тестов. Дешифрация диагностических экспериментов

Ubar, Raimund-Johannes 1981 https://www.ester.ee/record=b1326795*est