

Hybrid protection of digital FIR filters

Aksoy, Levent; Nguyen, Quang-Linh; **Almeida, Felipe**; **Raik, Jaan**; Flottes, Marie-Lise; Dupuis, Sophie; **Pagliarini, Samuel Nascimento** IEEE transactions on Very Large Scale Integration (VLSI) Systems 2023 / p. 812-825 : ill
<https://doi.org/10.1109/TVLSI.2023.3253641> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Logic IP for low-cost IC design in advanced CMOS nodes

Isgenc, Mehmet Meric; Martins, Mayler G.A.; Zackriya, V. Mohammed; **Pagliarini, Samuel Nascimento**; Pileggi, Larry IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2020 / p. 585-595 <https://doi.org/10.1109/TVLSI.2019.2942825>

Polymorphic configuration architecture for CGRAs

Jafri, Syed Mohammad Asad Hassan; **Tajammul, Muhammad Adeel**; Hermani, Ahmed; Paul, Kolin; Plosila, Juha; **Ellervee, Peeter**; Tenhunen, Hannu IEEE transactions on Very Large Scale Integration (VLSI) Systems 2016 / p. 403-407 : ill
<http://dx.doi.org/10.1109/TVLSI.2015.2402392>

RESAA: A Removal and Structural Analysis Attack Against Compound Logic Locking

Almeida, Felipe; **Aksoy, Levent**; **Pagliarini, Samuel Nascimento** IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2025 / p. 1348-1360 <https://doi.org/10.1109/TVLSI.2025.3534658>