

An agent-oriented method for designing large socio-technical service-ecosystems

Norta, Alexander; Mahunnah, Msury; Tenso, Tanel; Taveter, Kuldar; Narendra, Nanjangud C. 2014 IEEE Tenth World Congress on Services : SERVICES 2014 : 27 June-2 July 2014, Anchorage, Alaska : proceedings 2014 / p. 242-249 : ill

An educational environment for digital testing : hardware, tools, and web-based runtime platform

Jutman, Artur; Raik, Jaan; Ubar, Raimund-Johannes; Vislogubov, Vladislav Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 412-419 : ill

An external test approach for network-on-a-chip switches

Raik, Jaan; Govind, Vineeth; Ubar, Raimund-Johannes ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill <http://dx.doi.org/10.1109/ATS.2006.23>

Asynchronous fault detection in IEEE P1687 instrument network

Shibin, Konstantin; Devadze, Sergei; Jutman, Artur IEEE 23rd North Atlantic Test Workshop : 14-16 May 2014, Binghampton, New York : proceedings 2014 / p. 73-78 : ill

Back-traced deductive-parallel fault simulation for digital systems

Hahanov, Vladimir; **Ubar, Raimund-Johannes;** Hyduke, Stanley Proceedings : Euromicro Symposium on Digital System Design : Belek-Antalya, Turkey, September 1st to 6th, 2003 2003 / p. 370-377 : ill

Can a HW development and research environment be convenient, scalable and free? zamiaCAD : open-source platform for hardware design and analysis : [invited talk]

Jenihhin, Maksim Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 2012 / p. 548-549

Combined model of smart cities and electronic payments

Soe, Ralf-Martin; Mikheeva, Olga Proceedings of the 7th International Conference for E-Democracy and Open Government CeDEM17 : Danube University Krems, Krems, Austria, 17-19 May 2017 2017 / p. 194-205 : ill <https://doi.org/10.1109/CeDEM.2017.11>

Combining dynamic slicing and mutation operators for ESL correction

Repinski, Urmaz; Hantson, Hanno; Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / [6] p. : ill

Combining fault analysis technologies for ISO26262 functional safety verification

Augusto da Silva, Felipe; **Bagbaba, Ahmet Cagri;** Hamdioui, Said; Sauer, Christian 2019 IEEE 28th Asian Test Symposium (ATS) : 10-13 December 2019, Kolkata, India : proceedings 2019 / p. 129-134 : ill <https://doi.org/10.1109/ATS47505.2019.00024>

Comparison of model-based error localization algorithms for C designs

Repinski, Urmaz; Raik, Jaan Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 2012 / p. 42-45

Coordinated PI-based frequency deviation control of isolated hybrid microgrid : an online multi-agent tuning approach via reinforcement learning

Nosrati, Komeil; Tepljakov, Aleksei; Petlenkov, Eduard; Levron, Yoash; **Škiparev, Vjatseslav; Belikov, Juri** 2022 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe) : proceedings 2022 / p. 1-5 : ill <https://doi.org/10.1109/ISGT-Europe54678.2022.9960311>

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; Ubar, Raimund-Johannes; Devadze, Sergei; Raik, Jaan 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 108-113 : ill

Customizable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines : FCCM 2014 : 11-13 May 2014, Boston, Massachusetts, USA : proceedings 2014 / p. 31 : ill

Cycle-based simulation algorithms for digital systems using high-level decision diagrams

Morawiec, Adam; **Ubar, Raimund-Johannes; Raik, Jaan** Design, Automation and Test in Europe : Conference and Exhibition 2000 : Paris, France, March 27-30, 2000 : proceedings 2000 / p. 743

Cycle-based simulation with decision diagrams

Ubar, Raimund-Johannes; Morawiec, Adam; **Raik, Jaan** Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 454-458: ill

Defect-oriented fault simulation and test generation in digital circuits

Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE ISQED 2001 : proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design : March 26-28, 2001, San Jose, California 2001 / p. 365-371

Defect-oriented test- and layout-generation for standard-cell ASIC designs

Sudbrock, Joachim; **Raik, Jaan; Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill

Designing a contractual choreography language for automating cross-organizational business collaboration

Norta, Alexander; Ma, Lixin; Duan, Yucong 2014 IEEE Tenth World Congress on Services : SERVICES 2014 : 27 June-2 July 2014, Anchorage, Alaska : proceedings 2014 / p. 338-345 : ill

Developing multi-view Contracts using Event-B and Uppaal Timed Automata

Vain, Jüri; Tsiopoulos, Leonidas; Guin, Jishu 2016 21st International Conference on Engineering of Complex Computer Systems : ICECCS 2016 : Dubai, United Arab Emirates, 6-8 November 2016 : proceedings 2016 / p. 126-134 : ill
<https://doi.org/10.1109/ICECCS.2016.024>

Digital hardware organization course for SoC program

Ellervee, Peeter; Tenhunen, Hannu 2001 International Conference on Microelectronic Systems Education : June 17-18, 2001, Las Vegas, Nevada, USA : proceedings 2001 / p. 26-27

Digital work: A conceptual clarification

Baiyere, Abayomi; Schneider, Sabrina; **Stein, Mari-Klara** Proceedings of the Annual Hawaii International Conference on System Sciences 2023 / p. 4588-4597 <https://doi.org/10.125/103192>

Efficiency experiments on Hadoop and Giraph with PageRank

Koschel, Arne; Heine, Felix; **Astrova, Irina**; Korte, Fred; Rossow, Thomas; Stipkovic, Sebastian 24th Euromicro International Conference on Parallel, Distributed, and Network-Based Processing : PDP 2016 : 17-19 February 2016, Heraklion, Crete, Greece : proceedings 2016 / p. 328-331 : ill <https://doi.org/10.1109/PDP.2016.49>

Efficient hierarchical approach to test generation for digital systems

Ubar, Raimund-Johannes; Raik, Jaan IEEE ISQED 2000 : proceedings of the IEEE 2000 1st International Symposium on Quality Electronic Design : March 20-22, 2000, San Jose, California 2000 / p. 189-195 : ill

Embedded synthetic instruments for board-level testing

Jutman, Artur; Devadze, Sergei; Alekseyev, Igor; Wenzel, Thomas Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / 1 p. : ill

European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings

Cantarella, JD 2005 https://www.ester.ee/record=b2300865*est

Execution of dataflow process networks on OpenCL platforms

Lund, Wictor; Kanur, Sudeep; Ersfolk, Johan; **Tsiopoulos, Leonidas** 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing : PDP 2015 : 4-6 March 2015, Turku, Finland : proceedings 2015 / p. 618-625 : ill
<https://doi.org/10.1109/PDP.2015.29>

Experimental analysis of cost optimization for electrical floor heating systems in volatile energy markets

Uuemaa, Madis; Uleksin, Taaniel; Tammoja, Heiki 2017 International Conference on Control, Artificial Intelligence, Robotics & Optimization (ICCAIRO), 20-22 May 2017 : proceedings 2017 / p. 177-181 <http://doi.ieeecomputersociety.org/10.1109/ICCAIRO.2017.42>

Explaining the decisions of deep learning models for load disaggregation (NILM) based on XAI

Machlev, Ram; Malka, Asaf; Perl, Michael; Levron, Yoash; **Belikov, Yuri** 2022 IEEE Power & Energy Society General Meeting (PESGM) 2022 / art. 183865 , p. 1-5 : ill <https://doi.org/10.1109/PESGM48719.2022.9917049>

Fast test cost calculation for hybrid BIST in digital systems

Orasson, Elmet; Raidma, Rein; **Ubar, Raimund-Johannes; Jervan, Gert**; Peng, Zebo Euromicro Symposium on Digital Systems Design : [Architectures, Methods and Tools : DSD 2001] : September 4-6, 2001, Warsaw, Poland : proceedings 2001 / p. 318-325 : ill

Fault diagnosis in integrated circuits with BIST

Ubar, Raimund-Johannes; Kostin, Sergei; Raik, Jaan; Evertson, Teet; Lensen, Harri 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 604-610 : ill <http://dx.doi.org/10.1109/DSD.2007.4341530>

Fault-tolerant scheduling of mixed-critical applications on multi-processor platforms

Bagheri, Mehrdad; **Jervan, Gert** 2014 International Conference on Embedded and Ubiquitous Computing : EUC 2014 : 26-28

Formalization of finite state machines with data path for the verification of high-level synthesis

Borrione, Dominique; **Dušina, Julia**; Pierre, Laurence XI Brazilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil : proceedings 1998 / p. 99-102: ill

FP7 collaborative research project DIAMOND : diagnosis, error modeling and correction for reliable systems design

Raik, Jaan Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p
<https://ieeexplore.ieee.org/document/6233052>

Functional built-in self-test for processor cores in SoC

Ubar, Raimund-Johannes; Indus, Viljar; Kalmend, Oliver; Evertson, Teet; Orasson, Elmet 30th IEEE NORCHIP Conference : Copenhagen, Denmark, November 12-14, 2012 2012 / p. 1-4 : ill

Generation of tests for the localization of single gate design errors in combinational circuits using the stuck-at fault model

Ubar, Raimund-Johannes; Borrione, Dominique XI Brazilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil : proceedings 1998 / p. 51-54

Heuristics for designing and evaluating socio-technical agent-oriented behaviour models with Coloured Petri Nets

Mahunnah, Msury; Norta, Alexander; Ma, Lixin; Taveter, Kuldar IEEE 38th Annual International Computers, Software and Applications Conference Workshops : 27-29 July 2014, Västerås, Sweden : proceedings 2014 / p. 438-443 : ill

Hierarchical analysis of short defects between metal lines in CMOS IC

Pleskacz, Witold A.; **Jenihhin, Maksim; Raik, Jaan**; Rakowski, Michal; **Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw Proceedings : 11th EUROMICRO Conference on Digital System Design : Architectures, Methods and Tools : (DSD 2008) : September 3-5, 2008, Parma, Italy 2008 / p. 729-734 : ill

Hierarchical calculation of malicious faults for evaluating the fault-tolerance

Ubar, Raimund-Johannes; Devadze, Sergei; Jenihhin, Maksim; Raik, Jaan; Jervan, Gert; Ellervee, Peeter Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill

Hierarchical defect-oriented fault simulation for digital circuits

Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan; Ubar, Raimund-Johannes** IEEE European Test Workshop : 23-26 May 2000, Cascais, Portugal : ETW 2000 : proceedings 2000 / p. 69-74 : ill

Hierarchical identification of untestable faults in sequential circuits

Raik, Jaan; Ubar, Raimund-Johannes; Krivenko, Anna; Kruus, Margus 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 668-671 : ill
<http://dx.doi.org/10.1109/DSD.2007.4341539>

High-level decision diagram based fault models for targeting FSMs

Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill <http://dx.doi.org/10.1109/DSD.2006.60>

A hybrid BIST architecture and its optimization for SoC testing

Jervan, Gert; Peng, Zebo; Ubar, Raimund-Johannes; Kruus, Helena Proceedings of the 3rd International Symposium on Quality Electronic Design : ISQED 2002, March 18-21, 2002, San Jose, California 2002 / p. 273-279 : ill

Hybrid BIST optimization for core-based systems with test pattern broadcasting

Ubar, Raimund-Johannes; Jenihhin, Maksim; Jervan, Gert; Peng, Zebo DELTA 2004 : second IEEE International Workshop on Electronic Design, Test and Applications : 28-30 January 2004, Perth, Australia : proceedings 2004 / p. 3-8 : ill
<http://doi.ieeecomputersociety.org/10.1109/DELTA.2004.10057>

Hybrid BIST optimization using reseeding and test set compaction

Jervan, Gert; Orasson, Elmet; Kruus, Helena; Ubar, Raimund-Johannes 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 596-603 : ill
<http://dx.doi.org/10.1109/DSD.2007.4341529>

Hybrid BIST time minimization for core-based systems with STUMPS architecture

Jervan, Gert; Eles, Petru; Peng, Zebo; Ubar, Raimund-Johannes; Jenihhin, Maksim 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 3-5 November 2003, Boston, Massachusetts : proceedings 2003 / p. 225-232 : ill

IaaS platforms : how secure are they?

Astrova, Irina; Koschel, Arne; Henke, Mats Lennart IEEE 30th International Conference on Advanced Information Networking and

Applications Workshops : WAINA 2016 : 23-25 March 2016, Crans-Montana, Switzerland : proceedings 2016 / p. 843-848 : ill
<https://doi.org/10.1109/WAINA.2016.22>

Implementation of address-based data sorting on different FPGA platforms

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Ioulia Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 38-41

Improved fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

Information processing for mass-customized clothing production

Elbrecht, Pirjo; Palm, Knut-Joosep 2016 IEEE Tenth International Conference on Semantic Computing : 3-5 February 2016, Laguna Hills, California : proceedings 2016 / p. 362-365 : ill <https://doi.org/10.1109/ICSC.2016.51>

Integrated design and test generation under Internet based environment MOSCITO

Schneider, Andre; **Ivask, Eero; Ubar, Raimund-Johannes** Euromicro Symposium on Digital System Design : Architectures, Methods and Tools : September 4-6, 2002, Dortmund, Germany : proceedings 2002 / p. 187-194 : ill
<http://dx.doi.org/10.1109/DSD.2002.1115368>

Kalman-filter based maximum power point tracking for a single-stage grid-connected photovoltaic system

Farrokhi, Ehsan; Ghoreishy, Hoda; **Ahmadihangar, Roya; Rosin, Argo** IECON 2021 – 47th Annual Conference of the IEEE Industrial Electronics Society 2021 / Code 173927 <https://doi.org/10.1109/IECON48115.2021.9589653> [Conference Proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Measurement and operation based condition monitoring methodology for high voltage circuit breakers

Asefi, Sajjad; Andreesen, Guido; Leinakse, Madis; Kilter, Jako; Kalmet, Tauri; Manninen, Henri; Landsberg, Mart 2022 IEEE PES Innovative Smart Grid Technologies Conference Europe (ISGT-Europe) : proceedings 2022 / Art. 184786
<https://doi.org/10.1109/ISGT-Europe54678.2022.9960521>

Modelling sound conflict management for virtual-enterprise collaboration

Narendra, Nanjangud C.; **Norta, Alexander; Mahunnah, Msury;** Maggi, Fabrizio Maria 2014 IEEE International Conference on Services Computing SCC 2014 : 27 June-2 July 2014, Anchorage, Alaska : proceedings 2014 / p. 813-820 : ill

Morphable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; Tajammul, Muhammad Adeel; **Ellervee, Peeter** 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 42-49 : ill

Multi-level fault simulation of digital systems on decision diagrams

Ubar, Raimund-Johannes; Raik, Jaan; Ivask, Eero; Brik, Marina The First IEEE International Workshop on Electronic Design, Test and Applications : DELTA 2002, 29-31 January 2002, Christchurch, New Zealand : proceedings 2002 / p. 86-91 : ill

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams

Jasnetski, Artjom; **Raik, Jaan; Tšertov, Anton; Ubar, Raimund-Johannes** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

NoCDepend : a flexible and scalable dependability technique for 3D networks-on-chip

Hollstein, Thomas; Azad, Siavoosh Payandeh; Kogge, Thilo; Ying, Haoyuan; Hofmann, Klaus 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 75-78 : ill <http://dx.doi.org/10.1109/DDECS.2015.30>

Off-line testing of delay faults in NoC interconnects

Bengtsson, Tomas; **Jutman, Artur;** Kumar, Shashi; Peng, Zebo; **Ubar, Raimund-Johannes** 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 677-680 : ill <http://dx.doi.org/10.1109/DSD.2006.72>

Open data as enabler of public service co-creation : exploring the drivers and barriers

Toots, Maarja; McBride, Keegan David Braun; Kalvet, Tarmo; Krimmer, Robert Johannes Proceedings of the 7th International Conference for E-Democracy and Open Government CeDEM17 : Danube University Krems, Krems, Austria, 17-19 May 2017 2017 / p. 102-112 : tab <https://doi.org/10.1109/CeDEM.2017.12>

Optimization of memory-constrained hybrid BIST for testing core-based systems

Jervan, Gert; Kruus, Helena; Orasson, Elmet; Ubar, Raimund-Johannes Proceedings of the IEEE 2nd International Symposium on Industrial Embedded Systems : SIES'2007 : Lisbon, Portugal, 4-6 July 2007 2007 / p. 71-77

Power-constrained hybrid BIST test scheduling in an abort-on-first-fail test environment

He, Zhiyuan; **Jervan, Gert**; Peng, Zebo; Eles, Petru Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 83-86 : ill

Recognition and analysis of the contours drawn during the Poppelreuter's test

Nõmm, Sven; **Bardõš, Konstantin**; **Mašarov, Ilja**; **Kozhenkina, Julia**; Toomela, Aaro; Toomsoo, Toomas 2016 15th IEEE International Conference on Machine Learning and Applications : 18-20 December 2016, Anaheim, California : proceedings 2016 / p. 170-175 : ill <http://doi.org/10.1109/ICMLA.2016.0036>

A reference architecture for a national e-learning infrastructure

Saay, Mohammad Salim; **Norta, Alexander** 9th IEEE/ACM International Conference on Utility and Cloud Computing : UCC 2016 : 6-9 December 2016, Tongji University, Shanghai, China : proceedings 2016 / p. 404-409 : ill <https://doi.org/10.1145/2996890.3007894>

Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs

Pellerey, Francesco; **Jenihhin, Maksim**; Squillero, Giovanni; **Raik, Jaan**; Sonza Reorda, Matteo; **Tihomirov, Valentin**; **Ubar, Raimund-Johannes** 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill <https://doi.org/10.1109/ATS.2016.57>

Remote and virtual laboratories in problem-based learning scenarios

Wuttke, Heinz-Dietrich; **Ubar, Raimund-Johannes**; Henke, Karsten 2010 IEEE International Symposium on Multimedia ISM 2010 : 13-15 December 2010, Taichung, Taiwan : proceedings 2010 / p. 377-382 : ill <http://dx.doi.org/10.1109/ISM.2010.63>

Re-using chip level DFT at board level

Gu, Xinli; **Jutman, Artur** Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th–June 1st, 2012, Annecy, France 2012 / 1 p

Revolver : a high-performance MIMD architecture for collision free computing

Öberg, I.; **Ellervee, Peeter** Euromicro Conference : proceedings : 24th Euromicro Conference : Västerås, Sweden, August 25-27, 1998. Vol. 1 1998 / p. 301-308

RFID-based communications for a self-organizing robot swarm

Tammet, Tanel; **Vain, Jüri**; **Puusepp, Andres**; **Reilent, Enar**; **Kuusik, Alar** SASO 2008 : Second IEEE International Conference on Self-Adaptive and Self-Organizing Systems : 20-24 October, 2008, Venice, Italy : proceedings 2008 / p. 45-54

Sequential circuit test generation using decision diagram models

Raik, Jaan; **Ubar, Raimund-Johannes** Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 736-740: ill

Series buck-boost partial power converter based on the push-pull converter

Abdel-Rahim, Omar; **Chub, Andrii**; **Blinov, Andrei**; **Vinnikov, Dmitri** IECON 2022 : 48th Annual Conference of the IEEE Industrial Electronics Society : 17-20 Oct. 2022 2022 / code. 184962 <https://doi.org/10.1109/IECON49645.2022.9968574> [Conference Proceedings at Scopus](#) [Article at Scopus](#)

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic

Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

SSBDDs and double topology for multiple fault reasoning

Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 23-28

SystemC-based loose models for simulation speed-up by abstraction of RTL IP cores

Abrar, Syed Saif; **Jenihhin, Maksim**; **Raik, Jaan** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 71-74 : ill <http://dx.doi.org/10.1109/DDECS.2015.39>

Teaching digital system test

Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Kruus, Margus** The 27th EAAEIE Annual Conference : June 7-9, 2017, Grenoble 2017 / [6] p

Temporally extended high-level decision diagrams for PSL assertions simulation

Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill

Test cost minimization for hybrid BIST

Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes** IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 25-27 October 2000, Yamanashi, Japan : proceedings 2000 / p. 283-298 : ill

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes; Jenihhin, Maksim** 12th Asian Test Symposium (ATS 2003) : 17-19 November 2003, Xian, China 2003 / p. 318-325 : ill

The role of governance, cooperation, and eService use in current eGovernment stage models

Meyerhoff Nielsen, Morten Proceedings of the 49th Annual Hawaii International Conference on System Sciences : 5-8 January 2016, Kauai, Hawaii 2016 / p. 2850-2860 : tab <https://doi.org/10.1109/HICSS.2016.357>

Timing analysis in OO system life-cycles

Mötus, Leo; Näks, Tõnu; Holt, Jon D. Proceedings : First International Symposium on Object-Oriented Real-Time Distributed Computing (ISORC'98) : April 20-22, 1998, Kyoto, Japan 1998 / p. 327-334

Timing simulation of digital circuits with binary decision diagrams

Ubar, Raimund-Johannes; Jutman, Artur; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill

TOP : an algorithm for three-level optimization of PLDs

Dubrova, E.; **Ellervee, Peeter;** Miller, D.M.; Muzio, J.C. Design, Automation and Test in Europe : Conference and Exhibition 2000 : Paris, France, March 27-30, 2000 : proceedings 2000 / p. 751

Verified multiple-time signature scheme from one-time signatures and timestamping

Firsov, Denis; Lakk, Henri; Truu, Ahto 2021 IEEE 34th Computer Security Foundations Symposium (CSF) : June 21-25, 2021, Virtual Conference : proceedings 2021 / 13 p <https://doi.org/10.1109/CSF51468.2021.00051>

Verifying response times in networked automation systems using jitter bounds

Srinivasan, Seshadhri; **Vain, Jüri** IEEE 25th International Symposium on Software Reliability Engineering Workshops : ISSREW 2014 : 3-6 November 2014, Naples, Italy : proceedings 2014 / p. 47-50 : ill

Vulnerability assessment of web services with model-based mutation testing

Siavashi, Faezeh; Truscan, Dragos; **Vain, Jüri** 2018 IEEE 18th International Conference on Software Quality, Reliability, and Security - QRS 2018 - : 16-20 July 2018, Lisbon, Portugal : proceedings 2018 / p. 301-312 : ill <http://doi.org/10.1109/QRS.2018.00043>