

Hierarchical temporal memory implementation on FPGA using LFSR based spatial pooler

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A scalable technique to identify true critical paths in sequential circuits

Ubar, Raimund-Johannes; Kostin, Sergei; Jenihhin, Maksim; Raik, Jaan Proceedings 2017 IEEE 20th International Symposium on Design and Diagnostics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 152-157 : ill <https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553>