

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs

Jürimägi, Lembit; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan Microprocessors and microsystems 2020 / art. 103117, 12 p <https://doi.org/10.1016/j.micpro.2020.103117> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

High-level test generation for processing elements in many-core systems

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Azad, Siavoosh Payandeh; Raik, Jaan 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill <http://dx.doi.org/10.1109/ReCoSoC.2017.8016156>

Implementation-independent functional test generation for RISC microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Raik, Jaan VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 82-87 : ill <https://doi.org/10.1109/VLSI-SoC.2019.8920323>

Mixed-level identification of fault redundancy in microprocessors

Oyeniran, Adeboye Stephen; Ubar, Raimund-Johannes; Jenihhin, Maksim; Gürsoy, Cemil Cem; Raik, Jaan LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill <https://doi.org/10.1109/LATW.2019.8704591>

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits

Ubar, Raimund-Johannes; Jürimägi, Lembit; Oyeniran, Adeboye Stephen; Jenihhin, Maksim Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill <https://doi.org/10.1109/DSD.2019.00077>