A new approach to build a low-level malicious fault list starting from high-level description and alternative graphs
Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza, M.; **Ubar, Raimund-Johannes** Proceedings IEEE European Design & Test Conference, Paris, March 17-20, 1997 1997 / p. 560-565 https://ieeexplore.ieee.org/document/582417

A new evolutionary-technique-based approach to optimize pseudo-random TPG for logic BIST
Jutman, Artur; Aleksejev, Jevgeni; **Ubar, Raimund-Johannes** MEET/MARIND'2002 : proceedings of First International Congress on Mechanical and Electrical Engineering and Technology and Fourth International Conference on Marine Industry, 07-11 October 2002, Varna Bulgaria. Volume 1 2002 / p. 247-252 : ill

A new testability calculation method to guide RTL test generation
Raik, Jaan; **Nõmmeots, Tanel**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2005 / p. 71-82 : ill https://doi.org/10.1007/s10836-005-5288-5

A PC-based CAD system for training digital test
Ubar, Raimund-Johannes; **Buldas, Ahto**; Paomets, Priidu; Raik, Jaan; **Tulit, Viljar** The Fifth EUROCHIP Workshop on VLSI Design Training, 17-18-19 October 1994, Dresden, Germany 1994 / p. 152-157: ill

A scalable static test set compaction method for sequential circuits
Aleksejev, Igor; **Raik, Jaan**; **Jutman, Artur**; **Ubar, Raimund-Johannes** Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 87-92 : ill

A tool for advanced learning of LFSR-based testing principles
Jutman, Artur; **Tšertov, Anton**; **Ubar, Raimund-Johannes** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 175-178 : ill

A tool for teaching pseudo-random TPG principles
Jutman, Artur; **Tšertov, Anton**; **Ubar, Raimund-Johannes** Proceedings of the 17th EAEEIE Annual Conference on Innovation in Education for Electrical and Information Engineering : Craiova, Romania, June 1st-3rd, 2006 2006 / p. 182-187 : ill

Aastad, mis möödusid linnulennul
Ubar, Raimund-Johannes Raimund-Johannes Ubar. Bibliograafia 2016 / lk. 13-44 : ill., fot

About robustness of test patterns regarding multiple faults
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / p. 86-91 : ill https://www.infona.pl/resource/bwmeta1.element.ieee-art-000006261243

About the fragility of truth in the dialogue between science and society
Ubar, Raimund-Johannes Estonian Academy of Sciences year book = Annales Academiae Scientiarum Estonicae 2017 2018 / p. 58-60 https://www.ester.ee/record=b1874722*est

Accurate dialysis dose evaluation and extrapolation algorithms during online optical dialysis monitoring
Fridolin, Ivo; **Karai, Deniss**; **Kostin, Sergei**; **Ubar, Raimund-Johannes** IEEE transactions on biomedical engineering 2013 / p. 1371-1377 : ill https://doi.org/10.1109/TBME.2012.2234458 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Accurate NBTI-induced gate delay modeling based on intensive SPICE simulations
Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 21-26 : ill

Action-based learning system for teaching digital electronics and test
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 3rd European Workshop on Microelectronics Education : France, May 18AMP19, 2000 2000 / p. 107-110 : ill

Advanced technical education in the age of cyber physical systems
Vierhaus, Heinrich Theodor; Schölzel, Mario; **Raik, Jaan**; **Ubar, Raimund-Johannes** 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 193-198 : ill

Akadeemia hädad ja Eesti Teadusfond
Ubar, Raimund-Johannes; Martinson, Helle Kultuurileht 1994 / 6. mai, lk. 6

Akadeemik Raimund-Johannes Ubari peokõne "Kõrgharidus on võime näha puude taga metsa" : [Tallinna Tehnikaülikooli 90. aastapäeva pidulikul koosolekul 17. septembril 2008 TTÜ aulas]
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2008 2009 / lk. 138-142

Akadeemilisest tagasisidest ja teaduseusust
Ubar, Raimund-Johannes Postimees 1994 / 11. juuli

Akadeemilisest vabadusest ja riisiterast
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2013 2014 / lk. 11-21

Algorithm for restructuring of structurally synthesized BDDs
Jürimägi, Lembit; **Ubar, Raimund-Johannes** 2019 IEEE 31st International Conference on Microelectronics : Niš, Serbia September 16th-18th, 2019 : proceedings 2019 / p. 239-242 : ill https://doi.org/10.1109/MIEL.2019.8889578

Algorithms for hierarchical fault simulation in digital systems
Ubar, Raimund-Johannes; **Raik, Jaan**; Klüver, B. Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 530-535 : ill

Algorithms of functional level testability analysis for digital circuits
Ubar, Raimund-Johannes; Kuchcinski, Ktzysztof Periodica polytechnica. Electrical engineering 1992 / 3/4, p. 295-308

Alma mater! Quo vadis?
Ubar, Raimund-Johannes Jaunais Inseneris 1993 / nr. 4, 8. okt

Alternatiivsete graafide mudel loogikalülituste funktsioonide kirjeldamiseks ja analüüsiks
Anton, E.; **Ubar, Raimund-Johannes** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 42-43 https://www.ester.ee/record=b2449987*est

Alternative graph based test design in digital systems
Ubar, Raimund-Johannes Proceedings of 11. NORCHIP seminar, Trondheim, Nov. 9-10, 1993 1993 / p. 48-62

Alternative graphs and test pattern design in digital systems
Ubar, Raimund-Johannes Proc. of the 6th Workshop on New Directions for Testing, Montreal, Canada, May 20-22, 1992 1992

Alternative graphs as a mathematical tool and knowledge representation for diagnosis purposes in digital systems
Ubar, Raimund-Johannes BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 285-292: ill

An approach for PSL assertion coverage analysis with high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Shchenova, Tatjana** Proceedings of IEEE East-West Design & Test Symposium (EWDTS'10) : St. Petersburg, Russia, September 17-20, 2010 2010 / p. 13-16 : ill
https://ieeexplore.ieee.org/document/5742048

An approach for verification assertions reuse in RTL test pattern generation
Jenihhin, Maksim; **Raik, Jaan**; Fujiwara, Hideo; **Ubar, Raimund-Johannes**; **Viilukas, Taavi** Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTLT'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

An educational environment for digital testing : hardware, tools, and web-based runtime platform
Jutman, Artur; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Vislogubov, Vladislav Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 412-419 : ill https://www.researchgate.net/profile/Artur-Jutman/publication/220880167_An_Educational_Environment_for_Digital_Testing_Hardware_Tools_and_Web-Based_Runtime_Platform/links/02e7e53c3c71b0b2a7000000/An-Educational-Environment-for-Digital-Testing-Hardware-Tools-and-Web-Based-Runtime-Platform.pdf

An external test approach for network-on-a-chip switches
Raik, Jaan; **Govind, Vineeth**; **Ubar, Raimund-Johannes** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 185-190 : ill

An external test approach for network-on-a-chip switches
Raik, Jaan; **Govind, Vineeth**; **Ubar, Raimund-Johannes** ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill http://dx.doi.org/10.1109/ATS.2006.23

Analysis of a test method for delay faults in NoC interconnects
Bengtsson, Tomas; **Jutman, Artur**; Kumar, Shashi; **Ubar, Raimund-Johannes**; Peng, Zebo Proceedings of the IEEE East-West Design & Test Workshop (EWDTW'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 42-46 : ill

Applets for learning digital design and test [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Kruus, Margus**; Wuttke, Heinz-Dietrich 1st International Conference on Interactive Mobile and Computer Aided Learning (IMCL2006) : Amman, Jordan, April 19-21, 2006 2006 / p. 1-4 : ill. [CD-ROM]

Application of high-level decision diagrams for simulation-based verification tasks
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Estonian journal of engineering 2010 / 1, p. 56-77 : ill

Application of sequential test set compaction to LFSR reseeding
Aleksejev, Igor; **Jutman, Artur**; **Raik, Jaan**; **Ubar, Raimund-Johannes** 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 102-107 : ill http://dx.doi.org/10.1109/NORCHP.2008.4738292

Application of structurally synthesized binary decision diagrams for timing simulation of digital circuits
Jutman, Artur; **Ubar, Raimund-Johannes** Proceedings of the Estonian Academy of Sciences. Engineering 2001 / 4, p. 269-288 : ill

Application specific true critical paths identification in sequential circuits
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan**; **Devadze, Sergei**; **Oyeniran, Adeboye Stephen** 2019 IEEE 25th International Symposium on On-Line Testing and Robust System Design (IOLTS 2019) : 1-3 July 2019, Greece 2019 / p. 299-304 : ill https://doi.org/10.1109/IOLTS.2019.8854442

An approach for verification assertions reuse 2 in RTL test pattern generation
Jenihhin, Maksim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Viilukas, Taavi**; Fujiwara, Hideo Journal of Shanghai Normal University : Natural Sciences 2010 / p. 441-447 : ill
https://www.researchgate.net/publication/240613999_An_Approach_for_Verification_Assertions_Reuse_in_RTL_Test_Pattern_Generation

An approach to system-level design for test
Jervan, Gert; **Ubar, Raimund-Johannes**; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 121-149 : ill

APRICOT : a framework for teaching digital systems verification
Raik, Jaan; **Jenihhin, Maksim**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 172-177 : ill
http://dx.doi.org/10.1109/EAEEIE.2008.4610181

Arvamusi akadeemikutelt : teadustulemused, hinnangud ja ettepanekud : [arvamust avaldavad Jüri Engelbrecht, Ülo Lille, Boris Tamm, Mihkel Veiderma, Valdek Kulbach, Rein Küttner, Raimund-Johannes Ubar jt.]
Engelbrecht, Jüri; **Lille, Ülo**; **Tamm, Boris, inform.**; **Veiderma, Mihkel**; **Kulbach, Valdek**; **Küttner, Rein**; **Ubar, Raimund-Johannes** Eesti Teaduste Akadeemia aastaraamat 1997 1998 / lk. 121-143

Arvamusi akadeemikutelt ["kuumade teemade" kohta oma erialal]
Küttner, Rein; **Lille, Ülo**; **Saarma, Mart**; **Tamm, Boris, inform.**; **Ubar, Raimund-Johannes**; **Veiderma, Mihkel**; **Engelbrecht, Jüri** Eesti Teaduste Akadeemia aastaraamat 1998 1999 / lk. 148-171

Arvamusi akadeemikutelt [oluliste teadusprobleemide kohta]
Küttner, Rein; **Lille, Ülo**; **Ubar, Raimund-Johannes**; **Veiderma, Mihkel**; **Öpik, Ilmar**; **Engelbrecht, Jüri** Eesti Teaduste Akadeemia aastaraamat 1999 2000 / lk. 137-174

Arvamusi akadeemikutelt [oluliste teadusprobleemide kohta]
Engelbrecht, Jüri; **Kaljo, Dimitri**; **Krumm, Lembit**; **Mõtus, Leo**; **Tõugu, Enn**; **Ubar, Raimund-Johannes** Eesti Teaduste Akadeemia aastaraamat 2005 2006 / lk. 177-204. (Arvamusi akadeemikutelt)

Arvamusi akadeemikutelt [oluliste teadusprobleemide kohta]
Engelbrecht, Jüri; **Kaljo, Dimitri**; **Ubar, Raimund-Johannes** Eesti Teaduste Akadeemia aastaraamat = Annales academiae scientarum Estonicae 2013 2014 / lk. 258-273

Arvutid diagnoosivad arvuteid
Ubar, Raimund-Johannes Side. Raadio. Televisioon : infoseeria 10 1985 / lk. 6-10 https://www.ester.ee/record=b1232303*est

Arvutite diagnostika uurimissuuna kujunemisest Eestis
Ubar, Raimund-Johannes Kõrgema tehnilise hariduse ja tehnilise mõtte areng Eestis 1988 / lk. 110-127

Assembling low-level tests to high-level symbolic test frames
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings [of the] 15th NORCHIP Conference, Tallinn, 10-11 November 1997 1997 / p. 275-280: ill

Assertion checking with PSL and high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Digest of papers IEEE 8th Workshop on RTL and High Level Testing : WRTLT'07 : October 12-13, 2007, Beijing, China 2007 / p. 105-110 : ill

https://pld.ttu.ee/~maksim/phd_papers/%5B12%5D%20wrtlt%2707.pdf

Assessment of diagnostic test for automated bug localization
Tihhomirov, Valentin; **Tšepurov, Anton**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

Assessment of student's design results in e-learning-scenarios [Electronic resource]
Wuttke, Heinz-Dietrich; **Ubar, Raimund-Johannes**; Henke, Karsten; **Jutman, Artur** 8th International Conference on Technology Based Higher Education and Training : 10th to 13th July, 2007, KKR Hotel Kumamoto, Kumamoto, Japan : [proceedings] 2007 / [6] p. [CD-ROM]

Assotsiatsioon EUROCHIP avas ukse Tallinna Tehnikaülikoolile
Ubar, Raimund-Johannes Tehnikaülikool 1993 / 17. märts, lk. 1-2

Asynchronous e-learning resources for hardware design issues
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Proceedings of the International Conference on Computer Systems and Technologies (e-learning) : CompSysTech'04 : Rousse, Bulgaria, 17-18 June 2004 / p. IV.11-1 - IV.11-6 : ill https://www.researchgate.net/publication/234797327_Asynchronous_e-learning_resources_for_hardware_design_issues

At-speed functional built-in self-test methodology for processors [Electronic resource]
Ubar, Raimund-Johannes; **Indus, Viljar**; **Kalmend, Oliver** Proceedings of the IASTED International Conference on Engineering and Applied Science : December 27-29, 2012, Columbo, Sri Lanka 2012 / p. 168-172 : ill [CD-ROM]

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Devadze, Sergei**; **Raik, Jaan**; **Min, Mart** 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele
Gorev, Maksim 2015 https://digi.lib.ttu.ee/i/?3953

Aufstellung von Testfolgen für logische Schaltungen
Plakk, Mari; **Ubar, Raimund-Johannes** Internationales wissenschaftliches Kolloquium 1979 / S. 93-96
https://www.ester.ee/record=b2936968*est

Aukartus teaduse ees
Ubar, Raimund-Johannes Raimund-Johannes Ubar. Bibliograafia 2016 / lk. 47-56

Aukartus teaduse ees : [essee]. Nikolai Alumäe medal
Ubar, Raimund-Johannes Sirp 2014 / lk. 3-5 : fot https://www.sirp.ee/s1-artiklid/c21-teadus/aukartus-teaduse-ees/

Automated correction of design errors by edge redirection on high-level decision diagrams
Karputkin, Anton; **Ubar, Raimund-Johannes**; **Tombak, Mati**; **Raik, Jaan** 13th International Symposium on Quality Electronic Design (ISQED), 2012 2012 / p. 686-693 : ill https://ieeexplore.ieee.org/document/6113980

Automated design error debug using high-level decision diagrams and mutation operators
Raik, Jaan; **Repinski, Urmas**; **Tšepurov, Anton**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** Microprocessors and microsystems 2013 / p. 505-513 : ill https://doi.org/10.1016/j.micpro.2012.11.004 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Automated design error localization in RTL designs
Jenihhin, Maksim; **Tšepurov, Anton**; **Tihhomirov, Valentin**; **Raik, Jaan**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill https://doi.org/10.1109/MDAT.2013.2271420 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Automated software-based in-field self-test program synthesis
Jasnetski, Artjom; **Ubar, Raimund-Johannes**; **Tšertov, Anton** International journal of microelectronics and computer science 2017 / p. 57-64 : ill

Automated software-based self-test generation for microprocessors
Jasnetski, Artjom; **Ubar, Raimund-Johannes**; **Tšertov, Anton** Proceedings of the 24st International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2017 : Bydgoszcz, Poland, June 19-21, 2014 2017 / p. 453-458 : ill https://doi.org/10.23919/MIXDES.2017.8005252

Automated test bench generation for high-level synthesis flow ABELITE
Viilukas, Taavi; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Baranov, Samary Proceedings of IEEE East-West

Design & Test Symposium (EWDTS'2011) : Sevastopol, Ukraine, September 9-12, 2011 2011 / p. 13-16 : ill
https://ieeexplore.ieee.org/document/6116601

Automated test program synthesis for digital systems with high-level decision diagrams
Ubar, Raimund-Johannes Proc. of 7th International Conference 2005 / p. 171-180

Automatic diagnosis of simple design errors
Ubar, Raimund-Johannes; Borrione, Dominique Techniques of Informatics and Microelectronics for Computer Architecture 1999 / p. 91

Automatic diagnosis of simple design errors
Ubar, Raimund-Johannes; Borrione, Dominique TIMA annual report 1998 1999 / p. 97-98

Automatic generation of EFSMs and HLDDs for functional ATPG
Tšepurov, Anton; Guglielmo, Giuseppe di; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Viilukas, Taavi** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 143-146 : ill

Automatic SoC level test path synthesis based on partial functional models
Tšertov, Anton; **Ubar, Raimund-Johannes**; **Jutman, Artur**; **Devadze, Sergei** 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 https://ieeexplore.ieee.org/document/6114730

Automatic test generation system for VLSI
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 255-258

Avalik kiri Eesti elektrist : [Eesti elektrijaamade erastamisest NRG-le : Eesti Teaduste Akadeemia 36 akadeemiku pöördumine]
Aarna, Olav; **Lille, Ülo**; **Saarma, Mart**; **Saarma, Mart**; **Tamm, Boris, inform.**; **Ubar, Raimund-Johannes**; Ernits, Peeter; **Veiderma, Mihkel** Postimees 2001 / lk. 24 https://www.ester.ee/record=b1072778*est https://artiklid.elnet.ee/record=b2295176*est

Back-traced deductive-parallel fault simulation for digital systems
Hahanov, Vladimir; **Ubar, Raimund-Johannes**; Hyduke, Stanley Proceedings : Euromicro Symposium on Digital System Design : Belek-Antalya, Turkey, September 1st to 6th, 2003 2003 / p. 370-377 : ill https://ieeexplore.ieee.org/document/1231969

Back-tracing and event-driven techniques in high-level simulation with decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; Morawiec, Adam ISCAS 2000 Geneva : The 2000 IEEE International Symposium on Circuits and Systems : Emerging Technologies for the 21st Century : May 28-31, 2000 : proceedings. Vol. 1 2000 / p. I-208 - I-211
https://ieeexplore.ieee.org/document/857064

Balti Ülikoolide Sõprade Selts
Ubar, Raimund-Johannes Tehnikaülikool 1992 / 18. dets., lk. 2

BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia)
Rang, Toomas; **Min, Mart**; **Ubar, Raimund-Johannes** 1994

BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings
Rang, Toomas; **Min, Mart**; **Ubar, Raimund-Johannes** 1996 https://www.ester.ee/record=b2150914*est

Behavioral level modeling of digital systems for testing purposes
Ubar, Raimund-Johannes 42nd International Conference, Ilmenau, Germany, September 22-25, 1997. Part 1 1997 / p. 510-515

A benchmark suite for evaluating the efficiency of test tools
Kruus, Helena; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Gorev, Maksim**; **Pesonen, Vadim**; **Devadze, Sergei**; **Orasson, Elmet**; **Brik, Marina**; **Min, Mart**; **Annus, Paul**; **Kruus, Margus**; **Meigas, Kalju** BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 85-88 : ill

Berechnung von Booleschen Ableitungen bei der Testsatzanalyse für digitale Schaltungen
Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftlishe Zeitschrift für die gesamte elektronische Nachrichtentechnik 1977 / p. 21-23 : ill https://www.ester.ee/record=b1550811*est

Berechnung von tests für die Fehlerdiagnose in Digitalsystem
Ubar, Raimund-Johannes Internationales wissenschaftliches Kolloquium, 21. 1. November bis 5. November 1976, H. 2: Vortragsreihe A 2: Entwurf, Analyse und Einsatz von informationsverarbeitenden Systemen: IWK 1976 / p. [?]

Beschreibung digitaler Einrichtungen mit alternativen Graphen für die Fehlerdiagnose
Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftlishe Zeitschrift für die gesamte elektronische Nachrichtentechnik 1980 / p. 96-102 : ill https://www.ester.ee/record=b1550811*est

Bibliograafia : [Raimund-Johannes Ubar]
Raimund-Johannes Ubar. Bibliograafia 2016 / lk. [97]-243

BIST analyzer : a training platform for SoC testing [Electronic resource]
Jutman, Artur; **Tšertov, Anton**; **Tšepurov, Anton**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 37th Annual Frontiers in Education Conference : Global Engineering : Knowledge Without Borders, Opportunities Without Passports : Milwaukee, Wisconsin, October 10-13, 2007 2007 / p. S3H-8-S3H-13 : ill. [CD-ROM] http://dx.doi.org/10.1109/FIE.2007.4418125

Block-level fault model-free debug and diagnosis in digital systems
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of the 12th EUROMICRO Conference on Digital System Design, Architectures, Methods and Tools : Patras, Greece, August 27-29, 2009 2009 / p. 229-232 https://ieeexplore.ieee.org/document/5350128

Boolean derivatives and multi-valued simulation on binary decision diagrams
Ubar, Raimund-Johannes Proceedings of the 4th International Workshop Mixed Design of Integrated Circuits and Systems : MIXDES'97 : Poznan, Poland, 12-14 June 1997 1997 / p. 115-120

Boolean fault dignosis with structurally synthesized BDDs
Ubar, Raimund-Johannes Recent progress in the Boolean domain 2014 / p. 303-331 : ill

Bringing research issues into lab scenarios on the example of SoC testing [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International Conference on Engineering Education - ICEE 2007 : September 3-7, 2007, Coimbra, Portugal 2007 / [7] p. : ill. [CD-ROM]
http://icee2007.dei.uc.pt/proceedings/papers/429.pdf

Built-in self diagnosis with multiple signature analyzers in digital systems
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 29-34 : ill

CAD für Digitaltechnik - eine Programmfamilie für den Entwurf von Testmustern zum Test von Digitalschaltungen
Ubar, Raimund-Johannes IBM Hochschulkongress '92: Offene Grenzen - offene Systeme, Dresden, 30.09-2.10.1992 1992 / S.IV9 1-14

CAD software for digital test and diagnostics
Jervan, Gert; **Markus, Antti**; **Paomets, Priidu**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of International Conference on Design and Diagnostics of Electronic Circuits and Systems, Ostrava, Czech Republik, May 12-14, 1997 1997 / p. 35-40

A CAD system for teaching digital test
Ubar, Raimund-Johannes; **Ivask, Eero**; Paomets, Priidu; **Raik, Jaan** BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 369-372: ill

Calculation of LFSR seed and polynomial pair for BIST applications
Jutman, Artur; **Tšertov, Anton**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 105-108 : ill

Calculation of LFSR seed and polynomial pair for BIST applications [Electronic resource]
Jutman, Artur; **Tšertov, Anton**; **Ubar, Raimund-Johannes** 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 275-279 : ill. [CD-ROM] https://ieeexplore.ieee.org/abstract/document/4538801

Calculation of probabilistic testability measures for digital circuits with Structurally Synthesized BDDs
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** Microprocessors and microsystems 2020 / art. 103117, 12 p https://doi.org/10.1016/j.micpro.2020.103117 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Calculation of testability measures on structurally synthesized binary decision diagrams
Ubar, Raimund-Johannes; **Heinlaid, J.**; **Raik, Jaan**; Raun, L. BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 179-182: ill

Calculation of the diagnosibility of digital circuits without using fault models
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 159-162 : ill

Canonical representations of high-level decision diagrams
Karputkin, Anton; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Tombak, Mati** Estonian journal of engineering 2010 / 1, p. 39-55 : ill

Case study in testing digital systems
Ubar, Raimund-Johannes Baltic electronics 1995 / 1, p. 24-27

CEBE - Centre for Integrated Electronic Systems and Biomedical Engineering
Fridolin, Ivo; **Min, Mart**; **Ubar, Raimund-Johannes** The parliament magazine's research review : European research & innovation 2009 / p. 35

Centre for Integrated Electronic Systems and Biomedical Engineering - CEBE
Ubar, Raimund-Johannes Estonian journal of engineering 2010 / 1, p. 7-10 : ill

Challenges for future system-on-chip design
Hollstein, Thomas; Peng, Zebo; **Ubar, Raimund-Johannes**; Glesner, Manfred Circuit Paradigm in the 21st Century : ECCTD '01 : proceedings of the 15th European Conference on Circuit Theory and Design : Helsinki University of Technology, Finland, 28th-31st August 2001. Vol 3 2001 / p. 173-176

CMOS defects analysis using DefSim measurement environment
Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur**; **Ubar, Raimund-Johannes** Informal Digest of Papers : Eleventh IEEE European Test Symposium : ETS 2006 : 21-24 May 2006, Southampton, United Kingdom 2006 / p. 241-246 : ill

Code coverage analysis for concurrent programming languages using high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** Proceedings of the 12th European Workshop on Dependable Computing : EWDC 2009 : Toulouse, France, May 14-15, 2009 2009 / [4] p. : ill
https://hal.archives-ouvertes.fr/hal-00381559

Code coverage analysis using high-level decision diagrams [Electronic resource]
Raik, Jaan; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Ellervee, Peeter** 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 201-207 : ill. [CD-ROM]
https://ieeexplore.ieee.org/document/4538786

Collaborative distributed computing in the field of digital electronics testing
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Balanced Automation Systems for Future Manufacturing Networks : 9th IFIP WG 5.5 International Conference : BASYS 2010 : Valencia, Spain, July 21-23, 2010 : proceedings 2010 / p. 145-152

Collaborative distributed fault simulation for digital electronic circuits
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Intelligent Distributed Computing IV : proceedings of the 4th International Symposium on Intelligent Distributed Computing - IDC 2010 : Tangier, Morocco, September 2010 2010 / p. 67-76

Combinational fault simulation in sequential circuits
Ubar, Raimund-Johannes; **Kõusaar, Jaak**; **Gorev, Maksim**; **Devadze, Sergei** 2015 IEEE International Symposium on Circuits and Systems : 24-27 May 2015, Lisboa, Portugal : [proceedings] 2015 / p. 2876-2879 : ill https://doi.org/10.1109/ISCAS.2015.7169287
Conference proceedings at Scopus Article at Scopus Article at WOS

Combined fault-model free cause-effect and effect-cause fault diagnosis in block-level digital networks
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** ASQED'09 : 1st Asia Symposium on Quality Electronic Design : Kuala Lumpur, Malaisia, July 15-16, 2009 2009 / p. 385-390 https://ieeexplore.ieee.org/document/5206232

Combined pseudo-exhaustive and deterministic testing of array multipliers
Oyeniran, Adeboye Stephen; **Azad, Siavoosh Payandeh**; **Ubar, Raimund-Johannes** 2018 IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR) : THETA 21st edition, 24th-26th May, Cluj-Napoca, Romania : proceedings 2018 / 6 p. : ill https://doi.org/10.1109/AQTR.2018.8402708

Combining dynamic slicing and mutation operators for ESL correction
Repinski, Urmas; **Hantson, Hanno**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings : 2012 17th IEEE European Test Symposium (ETS) : May 28th-June 1st, 2012, Annecy, France 2012 / [6] p. : ill
https://ieeexplore.ieee.org/document/6233020

Combining functional and structural approaches in test generation for digital systems
Ubar, Raimund-Johannes Microelectronics reliability 1998 / p. 317-329 : ill https://doi.org/10.1016/S0026-2714(97)00192-3

Combining learning, training and research in laboratory course for design and test
Ubar, Raimund-Johannes; **Orasson, Elmet**; **Raik, Jaan**; Wuttke, Heinz-Dietrich The 7th Biennial Conference on Electronics and

Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 221-224 : ill
https://www.researchgate.net/publication/242397131_Combining_Learning_Training_and_Research_in_Laboratory_Course_for_Design_and_Test

Combining symbolic techniques with topological approach in test generation
Ubar, Raimund-Johannes Proceedings of the 3rd Workshop on Mixed Design of Integrated Circuits and Systems, Lodz, May 1996 1996 / p. 377-382

Compaction of decision diagrams for describing multi-process VHDL descriptions
Leveugle, R.; Saucier, Gabriele; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 195-198: ill

Comparative analysis of sequential circuit test generation approaches
Raik, Jaan; Krivenko, Anna; **Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 225-228 : ill

Comparison of genetic and random techniques for test pattern generation
Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 163-166: ill

Comparison of two approaches to improve functional BIST fault coverage
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Gorev, Maksim**; **Mägi, Gunnar** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 105-108 : ill

Complex delay fault reasoning with sequential 7-valued algebra
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Aleksejev, Igor** 2015 16th Latin American Test Symposium (LATS 2015) : Puerto Vallarta, Mexico, 25-27 March 2015 2015 / [6] p. : ill http://dx.doi.org/10.1109/LATW.2015.7102403

Computer-aided module-level text generation for digital devices on the basis of thin alternative graph-model
Pall, M.; Ubar, Raimund-Johannes Preprints the 2nd IFAC/IFIP Symposium on Software for Computer Control, SOCOCO, Prague, Czechoslovakia, June 11-15, 1979 ; Vol. 2 1979 / p. [?] https://www.ester.ee/record=b2041567*est

Conditional fault collapsing in digital circuits with shared structurally synthesized BDDs [Online resource]
Jürimägi, Lembit; **Ubar, Raimund-Johannes** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p. : ill https://doi.org/10.1109/BEC.2018.8600967

Constraint-based hierarchical untestability identification for synchronous sequential circuits
Raik, Jaan; **Rannaste, Anna**; **Jenihhin, Maksim**; **Viilukas, Taavi**; **Ubar, Raimund-Johannes**; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

Constraint-based hierarchical untestability identification for syncronous sequential circuits
Viilukas, Taavi; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Rannaste, Anna**; **Jenihhin, Maksim**; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Constraint-based test pattern generation at the register-transfer level
Viilukas, Taavi; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; **Krivenko, Anna** Proceedings of the 13th IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 14-16, 2010, Vienna, Austria 2010 / p. 352-357 : ill
http://dx.doi.org/10.1109/DDECS.2010.5491752

A constraint-driven gate-level test generator
Raik, Jaan; **Ubar, Raimund-Johannes**; **Jervan, Gert**; **Krupnova, Helena** BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 237-240: ill

Constraints analysis in hierarchical test generation for digital systems
Ubar, Raimund-Johannes; **Krupnova, Helena** BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 313-318: ill

Construction of the tests of combinational circuit failures by analyzing the orthogonal disjunctive normal forms represented by the alternative graphs
Matrosova, A.Yu.; Pleshkov, A.G.; **Ubar, Raimund-Johannes** Automation and remote control 2005 / p. 313-327 : ill
https://doi.org/10.1007/s10513-005-0054-9

Critical path tracing based simulation of transition delay faults

Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 61-66 : ill

Critical path tracing based simulation of transition delay faults
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 108-113 : ill

Cycle-based simulation algorithms for digital systems using high-level decision diagrams
Morawiec, Adam; **Ubar, Raimund-Johannes**; **Raik, Jaan** Design, Automation and Test in Europe : Conference and Exhibition 2000 : Paris, France, March 27-30, 2000 : proceedings 2000 / p. 743 https://ieeexplore.ieee.org/document/840876

Cycle-based simulation with decision diagrams
Ubar, Raimund-Johannes; Morawiec, Adam; **Raik, Jaan** Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 454-458: ill https://ieeexplore.ieee.org/document/761165

DECIDER : a decision diagram based hierarchical test generation system
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 269-273
https://www.ida.liu.se/labs/eslab/publications/pap/db/DDECS98.pdf

DECIDER : a system for hierarchical test pattern generation
Raik, Jaan; **Ubar, Raimund-Johannes** Radioelectronics and informatics 2003 / p. 40-45 : ill
https://www.researchgate.net/publication/250395975_DECIDER_A_System_for_Hierarchical_Test_Pattern_Generation

A decision diagram based hierarchical test pattern generator
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 159-162: ill

Decision diagrams - from a mathematical notion to engineering applications
Stankovic, Radomir S.; **Ubar, Raimund-Johannes**; Astola, Jaakko Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 281-301 : ill http://dx.doi.org/10.2298/FUEE1103281S

Decision diagrams and digital test
Ubar, Raimund-Johannes ECMS 2003 : 6th International Workshop on Electronics, Control, Measurment and Signals : Liberec, Czechia, June 2-4, 2003 2003 / p. 266-273 : ill http://www.midem-drustvo.si/Journal%20papers/MIDEM_35(2005)4p187.pdf

Decision diagrams and digital test
Ubar, Raimund-Johannes 41th International Conference on Microelectronics, Devices and Materials : MIDEM 2005 : Ribno at Bled, Slovenia : invited plenary paper 2005 / p. 15-26

Decision diagrams for diagnostic modeling
Ubar, Raimund-Johannes MEDIAN Finale : Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : November 10-11, 2015, Tallinn, Estonia 2015 / p. 43

Deductive fault simulation on structurally synthesized BDDs
Aarna, Margit; **Ubar, Raimund-Johannes**; **Raik, Jaan** BEC 2004 : Baltic Electronics Conference : Post-Graduate Student Session : Tallinn University of Technology, October 3-6, 2004, Tallinn, Estonia 2004 / p. 11 : ill

Defect oriented fault coverage of 100stuck-at fault test sets
Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 511-516 : ill https://repo.pw.edu.pl/info.seam?ps=20&id=WUT7e20f35d67ae45d3b2d1264d7a4ba722{=en&pn=1&cid=156607

Defect-oriented BIST quality analysis
Kruus, Helena; **Ubar, Raimund-Johannes**; **Raik, Jaan** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 153-156 : ill

Defect-oriented fault simulation and test generation in digital circuits
Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** IEEE ISQED 2001 : proceedings of the IEEE 2001 2nd International Symposium on Quality Electronic Design : March 26-28, 2001, San Jose, California 2001 / p. 365-371
https://ieeexplore.ieee.org/document/915257

Defect-oriented library builder and hierarchical test generation

Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 163-168 : ill

Defect-oriented mixed-level fault simulation in digital systems
Ubar, Raimund-Johannes; **Raik, Jaan**; **Ivask, Eero**; **Brik, Marina** Facta Universitatis [Niš]. Series electronics and energetics 2002 / 1, April, p. 123-136 : ill

Defect-oriented modul-level fault diagnosis in digital circuits
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 81-86

Defect-oriented test- and layout-generation for standard-cell ASIC designs
Sudbrock, Joachim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw; Pleskacz, Witold A. Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 79-82 : ill https://ieeexplore.ieee.org/document/1559781

Defect-oriented test generation and fault simulation in the environment of MOSCITO
Schneider, Andre; Diener, Karl-Heinz; Gramatova, Elena; Fisherova, Maria; **Ivask, Eero**; **Ubar, Raimund-Johannes**; Pleskacz, Witold A.; Kuzmicz, W. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 303-306 : ill

Defect-oriented test generation using probabilistic estimation
Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 131-136 : ill

Defects, faults and fault models
Gramatova, Elena; Fisherova, Maria; **Ubar, Raimund-Johannes**; Pleskacz, Witold A. Handbook of testing electronic systems 2005 / p. 26-96 : ill

DefSim - the defective IC
Pleskacz, Witold A.; **Jutman, Artur**; **Ubar, Raimund-Johannes**; **Devadze, Sergei** DATE 2007 : Design Automation and Test in Europe : Nice, France, April 16-20, 2007 2007 / p. s96 (2 p.)

DefSim: CMOS defects on chip for research and education
Pleskacz, Witold A.; Borejko, Tomasz; Walkanis, A.; Stopjakova, Viera; **Jutman, Artur**; **Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 74-79 : ill

DefSim: measurement environment for CMOS defects
Borejko, Tomasz; **Jutman, Artur**; Pleskacz, Witold A.; **Ubar, Raimund-Johannes** 2006 25th International Conference on Microelectronics : Belgrade, Serbia and Montenegro, 14-17 May 2006 : proceedings. Volume 2 2006 / p. 679-682 https://ieeexplore.ieee.org/document/1651048

DefSim-based exercises for studying defects in CMOS gates
Jutman, Artur; Pleskacz, Witold A.; **Boiko, Nikolai**; **Ubar, Raimund-Johannes** EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 23-26 : ill

Delay testing of asynchronous NoC interconnects
Bengtsson, Tomas; **Jutman, Artur**; Kumar, Shashi; **Ubar, Raimund-Johannes** Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 419-424 : ill

Department of Computer Engineering
Keevallik, Andres; **Ubar, Raimund-Johannes** Research activities / Tallinn Technical University 1993 / p. 75-78 https://www.ester.ee/record=b1053754*est

Dependability evaluation in fault-tolerant systems with high-level decision diagrams
Ubar, Raimund-Johannes; **Jervan, Gert**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ellervee, Peeter** Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 147-152 : ill https://www.db-thueringen.de/receive/dbt_mods_00008864

Description of digital objects with alternative graphs for test generation purposes
Ubar, Raimund-Johannes; **Lohuaru, Tõnu** Fault Tolerant Systems and Diagnostics : XI. International Conference ; Proceedings ; Suhl, June 6-9, 1988 1988 / p. [?]

Design and test technology for dependable systems-on-chip

2011 https://www.ester.ee/record=b4467408*est

Design error diagnosis in digital circuits with stuck-at fault model
Jutman, Artur; **Ubar, Raimund-Johannes** Microelectronics reliability 2000 / p. 307-320 : ill https://doi.org/10.1016/S0026-2714(99)00203-6

Design error diagnosis in digital circuits without error model
Ubar, Raimund-Johannes; Borrione, Dominique VLSI : systems on a chip : IFIP TC10 WG10.5 Tenth International Conference on Very Large Scale Integration (VLSI'99) : December 1-4, 1999, Lisboa, Portugal 1999 / p. 281-292 : ill https://www.researchgate.net/publication/292157544_Design_Error_Diagnosis_in_Digital_Circuits_without_Error_Model

Design error diagnosis in scan-path designs
Ubar, Raimund-Johannes 2nd IEEE Latin American Test Workshop : LATW 2001 : Cancun, Mexico, February 11-14, 2001 : digest of papers 2001 / p. 162-168 : ill

Design error diagnosis using backtrace algorithm on decision diagrams
Repinski, Urmas; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / p. 93-96

Design error diagnosis with re-synthesis in combinational circuits
Ubar, Raimund-Johannes Journal of electronic testing : theory and applications 2003 / 1, p. 73-82 : ill https://link.springer.com/article/10.1023/A:1021948013402

Design error localization in digital circuits by stuck-at fault test patterns
Jutman, Artur; **Ubar, Raimund-Johannes** [MIEL] 2000 : 22nd International Conference on Microelectronics : Niš, Yugoslavia, 14-17 May 2000 : proceedings. Volume 2 2000 / p. 723-726 https://ieeexplore.ieee.org/document/838792

Design technologies for system-on-chip : fault simulation in complex digital designs
Hahanov, V.; **Ubar, Raimund-Johannes** Автоматизированные системы управления и приборы автоматики, 2003 2003 / p. 16-35

Design-for-destability-based external test and diagnosis of mesh-like network- on-a-chips
Raik, Jaan; Govind, Vineeth; **Ubar, Raimund-Johannes** IET computers and digital techniques 2009 / 5, p. 476-486 : ill http://dx.doi.org/10.1049/iet-cdt.2008.0096

Deterministic defect-oriented test generation for combinational circuits
Raik, Jaan; **Ubar, Raimund-Johannes**; Sudbrock, Joachim; Kuzmicz, Wieslaw; Pleskacz, Witold A. LATW 2005 : 6th IEEE Latin-American Test Workshop : March 30 - April 2, 2005, Salvador, Bahia, Brazil : [digest of papers] 2005 / p. 325-330 : ill

DfT for application of external test patterns in a Network-on-a-Chip
Govind, Vineeth; **Raik, Jaan**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 25-28 : ill

Diagnosis and correction of multiple design errors using critical path tracing and mutation analysis
Hantson, Hanno; **Repinski, Urmas**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes** LATW 2012 : 13th IEEE Latin-American Test Workshop proceedings : April 10th-13th, 2012, Quito, Ecuador 2012 / [6 p.] : ill https://ieeexplore.ieee.org/document/6261234

Diagnostic modeling of digital systems with low- and high-level decision diagrams
Ubar, Raimund-Johannes LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [1] p

Diagnostic modeling of digital systems with multi-level decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Jutman, Artur**; **Jenihhin, Maksim** Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams

Diagnostic modeling of microprocessors with high-level decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Jutman, Artur**; **Jenihhin, Maksim**; **Brik, Marina**; Istenberg, Martin; Wuttke, Heinz-Dietrich BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 147-150 : ill

Diagnostic modelling of digital systems with binary and high-level decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Kruus, Helena**; **Lensen, Harri**; **Evartson, Teet** Progress in industrial mathematics at ECMI 2006 2008 / p. 902-907 : ill https://link.springer.com/chapter/10.1007/978-3-540-71992-2_158

Diagnostic modelling of digital systems with decision diagrams
Ubar, Raimund-Johannes Вестник Томского государственного университета : приложение 2004 / август, материалы международных, всесоюзных и региональных научных конференций, симпозиумов, школ, проводимых в ТГУ, с. 174-179 : ил

Diagnostic modelling of digital systems with multi-level decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Evartson, Teet**; **Kruus, Margus**; **Lensen, Harri** Proceedings of the 17th IASTED International Conference on Modelling and Simulation : May 24-26, 2006, Montreal, Quebec, Canada 2006 / p. 207-212 : ill

Diagnostic software
Ubar, Raimund-Johannes Concise encyclopedia of software engineering 1993 / p. 101-105

Diagnostic software with WEB interface for teaching purposes
Vislogubov, Vladislav; **Jutman, Artur**; **Kruus, Helena**; **Orasson, Elmet**; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 255-258 : ill

Diagnostic test generation for statistical bug localization using evolutionary computation
Gaudesi, Marco; **Jenihhin, Maksim**; **Raik, Jaan**; **Tihhomirov, Valentin**; **Ubar, Raimund-Johannes** Applications of Evolutionary Computation : 17th European Conference, EvoApplications 2014, Granada, Spain, April 23-25, 2014 : revised selected papers 2014 / p. 425-436 : ill https://doi.org/10.1007/978-3-662-45523-4_35 Conference proceeding at Scopus Article at Scopus Conference proceeding at WOS Article at WOS

DIAGNOZER : a laboratory tool for teaching research in diagnosis of electronic systems [Electronic resource]
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Jutman, Artur**; **Raik, Jaan**; Wuttke, Heinz-Dietrich 2009 IEEE International Conference on Microelectronic Systems Education MSE '09 : 25-27 July 2009, San Francisco, California : [proceedings] 2009 / p. 12-15 : ill. [CD-ROM] http://dx.doi.org/10.1109/MSE.2009.5270842

Digitaalarvutite operatsioonseadmed : õppevahend
Ubar, Raimund-Johannes 1978 https://www.ester.ee/record=b1313974*est

Digitaalsüsteemide diagnostika
Ubar, Raimund-Johannes 2005 http://www.ester.ee/record=b2097071*est

Digitaalsüsteemide diagnostika Tallinna Tehnikaülikoolis
Ubar, Raimund-Johannes Teadusmõte Eestis : tehnikateadused 2002 / lk. 107-113 : ill

Digital design flow with test activities
Diener, Karl-Heinz; Elst, G.; **Ivask, Eero**; **Jervan, Gert**; Peng, Z.; **Raik, Jaan**; **Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

Digital design learning system based on Java applets
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** 4th Annual Conference of the LTSN Centre for Information and Computer Sciences : 26th-28th August 2002, NUI Galway, Ireland 2003 / p. 183-187 : ill
https://pld.ttu.ee/dildis/publications/Sudnitson%20LTSN-ICS%202003.pdf

Digital electronics design and test at Computer Engineering Department of Tallinn University of Technology
Ubar, Raimund-Johannes; **Raik, Jaan**; **Jutman, Artur**; **Ellervee, Peeter** The house magazine : the parlamentary weekly 2006 / 1198, p. 42 : ill

Digital logic simulation with compressed BDDs
Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Devadze, Sergei**; **Raik, Jaan** Proceedings : 2011 IEEE International Conference on Computer Science and Automation Engineering : June 10-12, 2011, Shanghai, China 2011 / p. 105-109 : ill
https://ieeexplore.ieee.org/document/5952643

Digital test in WEB-based environment
Ivask, Eero 2006 https://www.ester.ee/record=b2158119*est

Distance learning tools for the field of electronics design and test
Ubar, Raimund-Johannes ITHET 2003 proceedings : 4th International Conference on Information Technology based Higher Education and Training : July 7-9, 2003, Marrakech, Morocco 2003 / p. 285-290 : ill

Distance-learning tools for digital design and test issues
Jutman, Artur; **Kruus, Margus**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** IT+SE'2002 : Information Tec[h]nologies in Science, Education, Telecommunication, Business : proceedings = Информационные технологии в науке, образовании, телекоммуникации, бизнесе, Украина, Крым, Ялта-Гурзуф, 20-30 мая 2002 года : труды 2002 / p. 269-272 : ill

Distributed approach for genetic test generation in the field of digital electronics

Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes** Intelligent Distributed Computing, Systems and Applications : proceedings of the 2nd International Symposium on Intelligent Distributed Computing : IDC 2008 : Catania, Italy, 2008 2008 / p. 127-136

Distributed approach for parallel exact critical path tracing fault simulation
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** MIXDES 2010 : 17th International Conference "Mixed Design of Integrated Circuits and Systems" : June 24-26, 2010, Wroclaw, Poland 2010 / p. 471-476 : ill

Distributed approach for parallel exact critical path tracing fault simulation
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** International journal of microelectronics and computer science 2010 / p. 165-174 : ill

Distributed fault simulation with collaborative load balancing for VLSI circuits
Ivask, Eero; **Devadze, Sergei**; **Ubar, Raimund-Johannes** Scalable computing : practice and experience 2011 / p. 153-163 : ill

Doktoritest ja professoritest
Ubar, Raimund-Johannes Tehnikaülikool 1993 / 17. märts, lk. 7 https://www.ester.ee/record=b5309277*est

DOT: new deterministic defect-oriented ATPG tool
Raik, Jaan; **Ubar, Raimund-Johannes**; Sudbrock, Joachim; Kuzmicz, Wieslaw; Pleskacz, Witold A. European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings 2005 / p. 96-101 : ill

Double phase fault collapsing with linear complexity in digital circuits
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Orasson, Elmet**; **Josifovska, Galina**; **Oyeniran, Adeboye Stephen** DSD 2015 : 18th Euromicro Conference on Digital Systems Design : 26-28 August 2015, Funchal, Madeira, Portugal 2015 / p. 700-705 : ill

Dynamic analysis of digital circuits with 5-valued simulation
Ubar, Raimund-Johannes Mixed design of integrated circuits and systems 1998 / p. 187-192: ill
https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_29

Dynamic analysis of digital circuits with multi-valued simulation
Ubar, Raimund-Johannes Microelectronics journal 1998 / 11, p. 821-826: ill

Education environment for electronics and microsystems
Ajaots, Maido; **Min, Mart**; **Rang, Toomas**; **Ubar, Raimund-Johannes** Microelectronics education : proceedings of the European Workshop, Grenoble, France, 5-6 Feb 1996 1996 / p. 145-148: ill

Education environment for electronics and microsystems
Ajaots, Maido; **Min, Mart**; **Rang, Toomas**; **Ubar, Raimund-Johannes** First European Workshop on Microelectronics Education, Villard de Lans, France, February 5-6, 1996 : proceedings 1996 / p. 39

EE : Eesti (Estonia)
Ubar, Raimund-Johannes; **Rüstern, Ennu**; **Kruus, Margus** Towards the harmonisation of Electrical and Information Engineering Education in Europe : 2003-2004 2003 / p. 67-74 : ill http://www.ester.ee/record=b2300874*est

Eesti kõrgharidus ja teadus pankrotiohus?
Ubar, Raimund-Johannes Kultuurileht 1995 / 20. jaan., lk. 6: ill

Eesti mikroelektroonika osaleb maailma virtuaalses kaubamajas
Ubar, Raimund-Johannes Eesti Päevaleht 1998 / 12. veebr., Uus Meedia, lk. 6

Eesti teaduse tippkeskus infotehnoloogia teaduskonda
Ubar, Raimund-Johannes; **Fridolin, Ivo**; **Min, Mart** Tallinna Tehnikaülikooli aastaraamat 2008 2009 / lk. 19-26

Eesti Teadusfond vastutab grantide eest
Ubar, Raimund-Johannes Eesti Päevaleht 1996 / 25. nov., lk. 6: ill

Eesti Vabariigi 1999. aasta tehnikateaduste [R.Ubarile antud] aastapreemia tagamaadest
Ubar, Raimund-Johannes Tehnikaülikool 1999 / 5. apr., lk. 4-5

Eestilt Euroopale : [Euroopa nanotehnika foorumil osales Eestist Raamprogrammi FP7 projekt DIAMOND, mida juhib TTÜ arvutitehnika instituudi professor Jaan Raik]
Ubar, Raimund-Johannes Mente et Manu 2012 / lk. 8 : fot https://www.ester.ee/record=b1242496*est

Eestis valmis üliväike hiiglane
Põldre, Jüri; **Ubar, Raimund-Johannes** Uus Meedia : Eesti Päevalehe lisa 1997 / 13. nov., lk. 6

Efficient hierarchical approach to test generation for digital systems
Ubar, Raimund-Johannes; **Raik, Jaan** IEEE ISQED 2000 : proceedings of the IEEE 2000 1st International Symposium on Quality Electronic Design : March 20-22, 2000, San Jose, California 2000 / p. 189-195 : ill https://ieeexplore.ieee.org/document/838873

Efficient single-pattern fault simulation on structurally synthesized BDDs
Raik, Jaan; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Jutman, Artur** Dependable Computing - EDCC-5 : 5th European Dependable Computing Conference : Budapest, Hungary, April 20-22, 2005 : proceedings 2005 / p. 332-344 : ill

Ein universeller Weg zur Automatisierung des Testentwurfs für digitale Objecte
Ubar, Raimund-Johannes; Lohuaru, Tõnu Fehler in Automaten 1989 / S. 16-30 : lll

E-learning environment for WEB-based study of testing
Ubar, Raimund-Johannes; **Jutman, Artur**; **Raik, Jaan**; **Devadze, Sergei**; **Jenihhin, Maksim**; **Aleksejev, Igor**; **Tšepurov, Anton**; **Tšertov, Anton**; **Kostin, Sergei**; **Orasson, Elmet**; Wuttke, Heinz-Dietrich Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 2010 / p. 47-52 : ill

E-learning environment in the area of digital microelectronics
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich ITHET 2004 : proceedings of the Fifth International Conference on Information Technology based Higher Education and Training : 31 May - 2 June, 2004, Istanbul, Turkey 2004 / p. 278-283 : ill

E-learning tool and excercises for teaching digital test
Ubar, Raimund-Johannes; **Orasson, Elmet** Proceedings of the 2nd IEEE Conference on Signals, Systems, Decision and Information Technology : Sousse, Tunisia, 2003 2003 / [6] p. : ill https://pld.ttu.ee/dildis/publications/E-Learning%20tool%20and%20Excercises.pdf

E-learning tool and excercises for teaching digital test
Ubar, Raimund-Johannes; **Orasson, Elmet** Proceedings of the 2nd IEEE Conference on Signals, Systems, Decision and Information Technology : Sousse, Tunisia, 2003 : summaries / p. 134

E-learning tools for digital test
Devadze, Sergei; Gorjachev, R.; **Jutman, Artur**; **Orasson, Elmet**; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** Proc. lll International Conference "Distance Learning - Educational Sphere of XXI Century" : Minsk, Belorussia, 2003 2003 / p. 336-342

E-learning tools for teaching self-test of digital electronics
Jutman, Artur; Gramatova, Elena; Pikula, T.; **Ubar, Raimund-Johannes** 15 EAEEIE International Conference on Innovation in Education for Electrical and Information Engineering : Sofia, Bulgaria, May 27-29, 2004 2004 / p. 267-272 : ill

Electronics Competence Centre at Tallinn Technical University
Ubar, Raimund-Johannes; **Vainomaa, Kaido** BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 597-602: ill https://www.ester.ee/record=b2150914*est

Electronics Competence Centre at the Tallinn Technical University
Ubar, Raimund-Johannes Baltic electronics 1995 / 2, p. 9-11

Electronics design and test
Ubar, Raimund-Johannes; **Kruus, Margus**; **Rang, Toomas** Public service review : European Union. 13 2007 / p. 52-53

Elektroonika ja arvutustehnika vabariiklikust sihtprogrammist
Ubar, Raimund-Johannes Arvutustehnika ja Andmetöötlus 1994 / 1, lk. 1-6

Elektroonika kompetentsuskeskus avas uksed kasutajatele Tallinna Tehnikaülikoolis
Ubar, Raimund-Johannes Tallinna Ülikoolid 1996 / 1. veebr., lk. 2-3: ill

Elektroonika kompetentsuskeskus Tallinna Tehnikaülikooli juures
Ubar, Raimund-Johannes Arvutustehnika ja Andmetöötlus 1994 / 2, lk. 33-36 ; 3, lk. 28-33

Elektroonika kompetentsuskeskus Tallinna Tehnikaülikoolis
Ubar, Raimund-Johannes Sõnumileht 1996 / 13. veebr., lk. 17

Elektroonika kompetentsuskeskusest Tallinna Tehnikaülikooli juures
Ubar, Raimund-Johannes Arvutustehnika ja Andmetöötlus 1996 / 1, lk. 2-4

Elektroonika kui Eesti innovatsioonisüsteemi infrastruktuur

Min, Mart; **Rang, Toomas**; **Ubar, Raimund-Johannes** Eesti teadlaste kongress, 11.-15. augustini 1996. a. Tallinnas : ettekannete kokkuvõtted 1996 / lk. 265 https://www.ester.ee/record=b1052731*est

Elektroonikadisaini uued paradigmad
Ubar, Raimund-Johannes A & A 1998 / 5, lk. 5-10

Elektroonikatööstuse 50 miljonit
Ubar, Raimund-Johannes Luup 1999 / 1, lk. 23-25: ill

Embedded diagnosis in digital systems
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** 2008 26th International Conference on Microelectronics : Niš, Serbia, 11-14 May 2008 : proceedings. Vol. 2 2008 / p. 421-424 : ill

Embedded fault diagnosis in digital systems with BIST
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Microprocessors and microsystems 2008 / 5/6, p. 279-287 : ill

Energy minimization for hybrid BIST in a system-on-chip test environment
Ubar, Raimund-Johannes; **Shchenova, Tatjana**; **Jervan, Gert**; Peng, Zebo European Test Symposium : ETS 2005 : 22-25 May 2005, Tallinn, Estonia : proceedings 2005 / p. 2-7 : ill

Enhancing hierarchical ATPG with a functional fault model for multiplexers [Electronic resource]
Raik, Jaan; **Ubar, Raimund-Johannes** 7th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 18-21, 2004, Stará Lesná, Slovakia : proceedings 2004 / p. 219-222 : ill. [CD-ROM] https://www.semanticscholar.org/paper/Enhancing-Hierarchical-Atpg-with-a-Functional-Fault-Raik-Ubar/b42e913ac070fd774df97bd644c4e6220704f8d4

Environment for FPGA-based fault emulation
Ellervee, Peeter; **Raik, Jaan**; **Tammemäe, Kalle**; **Ubar, Raimund-Johannes** Proceedings of the Estonian Academy of Sciences. Engineering 2006 / 3-2, p. 323-335 : ill

Environment for innovative university research training in the field of digital test
Oyeniran, Adeboye Stephen; **Ademilua, Tolulope**; **Kruus, Margus**; **Ubar, Raimund-Johannes** 2021 30th Annual Conference of the European Association for Education in Electrical and Information Engineering (EAEEIE) 2021 https://doi.org/10.1109/EAEEIE50507.2021.9531003

Environment for the analysis of functional self-test quality in digital systems
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Kruus, Helena**; **Aarna, Margit**; **Devadze, Sergei** Proceedings of the Estonian Academy of Sciences 2014 / p. 151-162 : ill https://artiklid.elnet.ee/record=b2673964*est https://doi.org/10.3176/proc.2014.2.05 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Equivalent transformations of structurally synthesized BDDs and applications
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Viies, Vladimir** 2019 8th Mediterranean Conference on Embedded Computing (MECO) 2019 / 6 p. : ill https://doi.org/10.1109/MECO.2019.8760283

Evolutionary approach to test generation for functional BIST
Skobtsov, Y.A.; Ivanov, D.E.; Skobtsov, V.Y.; **Ubar, Raimund-Johannes**; **Raik, Jaan** Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. 151-155 : ill https://artiklid.elnet.ee/record=b1018764*est

Evolutionary approach to the functional test generation for digital circuits
Skobtsov, Y.A.; Ivanov, D.E.; Skobtsov, V.Y.; **Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 229-232 : ill

Exact parallel critical path fault tracing to speed-up fault simulation in sequential circuits
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Kostin, Sergei**; **Devadze, Sergei**; **Raik, Jaan** International journal of microelectronics and computer science 2018 / p. 9−18 https://ijmcs.dmcs.pl/web/guest/vol.-9-no.-1 https://ijmcs.dmcs.pl/documents/10630/345460/IJMCS_1_2018_2.pdf

Exact static compaction of independent test sequences
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 315-318 : ill

Exact static compaction of sequential circuit tests using branch-and-bound and search state registration
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** ETW'02 : 7th IEEE European Test Workshop, Gorfu Greece, May 26-29, 2002 : informal digest 2002 / p. 19-20 https://www.researchgate.net/publication/250423148_Exact_Static_Compaction_of_Sequential_Circuit_Tests_Using_Branch_and-Bound_and_Search_State_Registration

Experimental comparison of different diagnosis algorithms in the BIST environment
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan**; **Kruus, Margus** Proceedings of the 16th IASTED International Conference on Applied Simulation and Modelling : August 29-31, 2007, Palma de Mallorca, Spain 2007 / p. 271-276 : ill
https://www.researchgate.net/publication/262275431_Experimental_comparison_of_different_diagnosis_algorithms_in_the_BIST_environment

Exploiting high-level descriptions for circuits fault tolerance assessments
Benso, A.; Prinetto, Paolo; Rebaudengo, M.; Sonza Reorda, Matteo; **Raik, Jaan**; **Ubar, Raimund-Johannes** 1997 IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, Paris, October 20-22, 1997 1997 / p. 212-216
https://ieeexplore.ieee.org/document/628327

Explorations in low area overhead DfT techniques for sequential BIST
Raik, Jaan; Raidma, Rein; **Ubar, Raimund-Johannes** IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 220-223 : ill

An external diagnosis method for network-on-a-chip
Raik, Jaan; Govind, Vineeth; **Ubar, Raimund-Johannes** IEEE/ACM Design Automation and Test in Europe, Workshop on Diagnostic Services in Networks-on-Chips - Test, Debug and On-line Monitoring : April 16-20, 2007, Nice, France 2007 / [2] p. : ill

Fast and efficient static compaction of test sequences based on greedy algorithms
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Győr, Hungary, April 18-20, 2001 2001 / p. 117-122 https://slideplayer.com/slide/9971880/#google_vignette

Fast and efficient static compaction of test sequences using bipartite graph representations
Markus, Antti; **Raik, Jaan**; **Ubar, Raimund-Johannes** ECS'99 : proceedings of the 2nd Electronic Circuits and Systems Conference : September 6-8, 1999, Bratislava, Slovakia 1999 / p. 17-20

Fast extended test access via JTAG and FPGAs
Devadze, Sergei; **Jutman, Artur**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes** International Test Conference 2009 : November 1 - November 6, 2009, Austin Convention Center, Austin, Texas USA : proceedings 2009 / p. 1-7 : ill
http://dx.doi.org/10.1109/TEST.2009.5355668

Fast fault emulation for synchronous sequential circuits
Raik, Jaan; **Ellervee, Peeter**; Tihhomirov, Valentin; **Ubar, Raimund-Johannes** Proceedings of East–West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 35-40
https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=a6eb712498a5f23db3f95ad66bada257c21e96f0

Fast fault simulation for extended class of faults in scan-path circuits
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** Proceedings : Fifth IEEE International Symposium on Electronic Design, Test and Applications : DELTA 2010 : 13-15 January 2010, Ho Chi Minh City, Vietnam 2010 / p. 14-19
https://ieeexplore.ieee.org/document/5438717

Fast identification of true critical paths in sequential circuits
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan**; **Jürimägi, Lembit** Microelectronics reliability 2018 / p. 252-261 : ill https://doi.org/10.1016/j.microrel.2017.11.027 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Fast RTL fault simulation using decision diagrams and bitwise set operations
Reinsalu, Uljana; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Ellervee, Peeter** 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170
https://ieeexplore.ieee.org/document/6104440

Fast static compaction of test sequences using implications and greedy search
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** ETW 2001 : IEEE European Test Workshop : Stockholm, May 29 June 1, 2001 : informal digest 2001 / p. 207-209 : ill https://www.semanticscholar.org/paper/Fast-Static-Compaction-of-Test-Sequences-using-and-Raik-Jutman/3a7a8ddda6e63d3e2fde0c8650d4518851746221

Fast static compaction of tests composed of independent sequences : basic properties and comparison of methods
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume II 2002 / p. 445-448 : ill
http://dx.doi.org/10.1109/ICECS.2002.1046190 https://ieeexplore.ieee.org/document/1046190

Fast test cost calculation for hybrid BIST in digital systems
Orasson, Elmet; Raidma, Rein; **Ubar, Raimund-Johannes**; **Jervan, Gert**; Peng, Zebo Euromicro Symposium on Digital Systems Design : [Architectures, Methods and Tools : DSD 2001] : September 4-6, 2001, Warsaw, Poland : proceedings 2001 / p. 318-325 : ill https://www.semanticscholar.org/paper/Fast-test-cost-calculation-for-hybrid-BIST-in-Orasson-Raidma/5aafcda5a18c2aabf0ad20cac10af10727f3c58f

Fast test pattern generation for sequential circuits using decision diagram representations
Raik, Jaan; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications (JETTA) 2000 / 3, p. 213-226 : ill
https://link.springer.com/article/10.1023/A:1008335130158

Fault collapsing in digital circuits using fast fault dominance and equivalence analysis with SSBDDs
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Orasson, Elmet**; **Raik, Jaan** VLSI-SoC : Design for Reliability, Security, and Low Power : 23rd IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2015 Daejeon, Korea, October 5-7, 2015 : revised selected papers 2016 / p. 23-45 : ill https://doi.org/10.1007/978-3-319-46097-0_2 Conference Proceedings at Scopus Article at Scopus Article at WOS

Fault collapsing with linear complexity in digital circuits
Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Raik, Jaan**; **Jutman, Artur** Proceedings of 2010 IEEE International Symposium on Circuits and Systems (ISCAS 2010) : 30 May - 2 June 2010, Paris, France 2010 / p. 653-656 : ill
https://ieeexplore.ieee.org/document/5537504

Fault diagnosis in integrated circuits with BIST
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan**; **Evartson, Teet**; **Lensen, Harri** 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 604-610 : ill http://dx.doi.org/10.1109/DSD.2007.4341530

Fault diagnosis in the BIST environment based on bisection of detected faults
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** LATW2007 : 8th IEEE Latin-American Test Workshop : March 11-14, 2007, Cuzco, Peru 2007 / [6] p. : ill

Fault diagnosis in VLSI devices
Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 1995 / 1, p. 51-67

Fault diagnosis of VLSI devices using alternative graph representation
Ubar, Raimund-Johannes Proceedings of the 8th Symposium on Microcomputer and Microprocessor Applications, Budapest, October 12-14, 1994. Vol. 1 1994 / p. 34-44

Fault effect reasoning in digital systems by topological view on low- and high-level decision diagrams
Ubar, Raimund-Johannes Вестник Томского государственного университета. Управление, вычислительная техника и информатика 2014 / p. 99-113 : ill http://journals.tsu.ru/informatics/&journal_page=archive&id=923&article_id=12107

Fault model and test synthesis for RISC-processors
Ubar, Raimund-Johannes; **Markus, Antti**; **Jervan, Gert**; **Raik, Jaan** BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 229-232: ill

Fault modeling and diagnosis in digital systems
Ubar, Raimund-Johannes CREDES Summer School : Dependable Systems Design : handouts 2011 / p. 91-106 : ill

Fault modeling and test generation with low- and high-level decision diagrams
Ubar, Raimund-Johannes 24. GI/GMM/ITG-Workshop : Testmethoden und Zuverlässigkeit von Schaltungen und Systemen 2012 / p. 1-12

Fault oriented test pattern generation for sequential circuits using genetic algorithms
Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes** IEEE European Test Workshop 2000 / p. 319-320

Fault oriented test pattern generation for sequential circuits using Genetic Algorithms
Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 129-132 : ill

Fault simulation of digital systems = Digitaalsüsteemide rikete simuleerimine
Devadze, Sergei 2009 https://digi.lib.ttu.ee/i/?445 https://www.ester.ee/record=b2508727*est

Fault simulation with parallel critical path tracing for combinational circuits using structurally synthesized BDDs
Devadze, Sergei; **Raik, Jaan**; **Jutman, Artur**; **Ubar, Raimund-Johannes** 7th IEEE Latin American Test Workshop LATW'06 : Buenos Aires, Argentina, March 26th-29th, 2006 : proceedings 2006 / p. 97-102 : ill

Fault simulation with parallel exact critical path tracing in multiple core environment
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Devadze, Sergei** 2015 Design, Automation & Test in Europe Conference & Exhibition (DATE) : proceedings 2015 / p. 1180-1185 : ill

Faults and fault models for integrated circuits and systems [Electronic resource] : [slides]

Ubar, Raimund-Johannes Design and Test Technology for Dependable Hardware/Software Systems : DEDIS/DAAD Summer Academy : BTU Cottbus, Sept. 1st-12th, 2008 2008 / [64] p. : ill. [CD-ROM]

Feasibility of structurally synthesized BDD models for test generation
Raik, Jaan; **Ubar, Raimund-Johannes** Proceedings of the IEEE European Test Workshop, Barcelona, Spain, May 27-29, 1998 1998 / p. 145-146

Fehler in Automaten
1989 http://www.ester.ee/record=b2015320*est

Fehlerbestimmung in kombinatorischen Scaltungen durch Lösung der Booleschen Differentialgleichungen
Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftlishe Zeitschrift für die gesamte elektronische Nachrichtentechnik 1978 / p. 330-334 : ill https://www.ester.ee/record=b1550811*est

Foreword
Rang, Toomas; **Min, Mart**; **Ubar, Raimund-Johannes** BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 3 https://www.ester.ee/record=b2150914*est

Foreword
Ubar, Raimund-Johannes; Prinetto, Paolo; Al-Hashimi, Bashir Informal Digest of Papers : 10 IEEE European Test Symposium : Tallinn, Estonia, May 22-25, 2005 2005 / p. III

Foreword to the 12th IEEE DDECS Symposium
Pliva, Zdenek; Manhaeve, Hans; Renovell, Michel; Novak, Ondrej; **Ubar, Raimund-Johannes**; Drabkova, Jindra Proceedings of the 2009 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 15-17, 2009, Liberec, Czech Republic 2009 / p. iii http://dx.doi.org/10.1109/DDECS.2009.5012081

Formal verification and error correction on high-level decision diagrams = Formaalne verifitseerimine ja vigade parandamine kõrgtasemelistel otsustusdiagrammidel
Karputkin, Anton 2012

FPGA based fault emulation of synchronous sequential circuits
Ellervee, Peeter; **Raik, Jaan**; Tihhomirov, Valentin; **Ubar, Raimund-Johannes** Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 59-62 https://ieeexplore.ieee.org/abstract/document/1423822

FPGA design flow with automated test generation
Elst, G.; Diener, Karl-Heinz; **Ivask, Eero**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proc. of German 11th Workshop on Test Technology and Reliability of Circuits and Systems : Potsdam, 1999 1999 / p. 120-123
https://masters.donntu.ru/2010/fknt/masyakin/library/article7.pdf

FPGA-based fault emulation of synchronous sequential circuits
Ellervee, Peeter; **Raik, Jaan**; **Tammemäe, Kalle**; **Ubar, Raimund-Johannes** IET computers and digital techniques 2007 / 2, p. 70-76 : ill https://ieeexplore.ieee.org/abstract/document/1423822

From online fault detection to fault management in network-on-chips : a ground-up approach
Azad, Siavoosh Payandeh; **Niazmand, Behrad**; **Janson, Karl**; **Nevin, George**; **Oyeniran, Adeboye Stephen**; **Putkaradze, Tsotne**; **Apneet Kaur**; **Raik, Jaan**; **Jervan, Gert**; **Ubar, Raimund-Johannes**; **Hollstein, Thomas** Proceedings 2017 IEEE 20th International Symposium on Design and Diagnotics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 48-53 : ill https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553

FTGEN - система генерирования функциональных тестов
Ubar, Raimund-Johannes; **Dušina, Julia**; **Zaugarov, Viktor**; Крупнова Е.; **Storožev, Sergei** Proceedings of CAD-93 : new information technologies for science, education and business, Yalta, May 4-13, 1993 1993 / p. 123-125

Functional built-in self-test for processor cores in SoC
Ubar, Raimund-Johannes; **Indus, Viljar**; **Kalmend, Oliver**; **Evartson, Teet**; **Orasson, Elmet** 30th IEEE NORCHIP Conference : Copenhagen, Denmark, November 12-14, 2012 2012 / p. 1-4 : ill https://ieeexplore.ieee.org/document/6403148

Functional level controllability analysis for digital circuits
Ubar, Raimund-Johannes; Kuchcinski, Ktzysztof Proc. of the Design Automation Conference, Kaunas, Lithuania, June 1-4, 1992 1992 / p. 13-21

Functional level test set generation methods
Ubar, Raimund-Johannes Proceedings of the 12th Conference on Fault-Tolerant Systems and Diagnostics, Prague, Czechoslovakia, September, 1989 1989 / p. 46-55

Functional level testability analysis for digital circuits
Ubar, Raimund-Johannes; Kuchcinski, Ktzysztof ETC '93 : European Test Conference, Rotterdam, The Netherlands, April 19-22, 1993 1993 / p. 545-546

Functional level testability analysis for digital circuits
Ubar, Raimund-Johannes 1992

Functional self-test of high-performance pipe-lined signal processing architectures
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Devadze, Sergei**; **Raik, Jaan**; **Min, Mart** Microprocessors and microsystems 2015 / p. 909-918 : ill https://doi.org/10.1016/j.micpro.2014.11.002 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Functional specification and testing of digital systems
Ubar, Raimund-Johannes Multimicroprocessor systems: Proceedings of the 3rd Symposium, Stralsund, oct. 16-20, 1989, Vol 1 1989 / p. 207-217

Functional test generation for finite state machines
Ubar, Raimund-Johannes; **Brik, Marina**; **Jutman, Artur**; **Raik, Jaan**; Bengtsson, Tomas; Kumar, Shashi BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 205-208 : ill

Functional test program generation for digital systems
Ubar, Raimund-Johannes; Dušina, Julia; **Krupnova, Helena**; **Storožev, Sergei**; **Zaugarov, Viktor** Testmethoden und Zuverlässigkeit von Schaltungen und Systemen : proceedings of the 6th workshop, Vaals (Niederlande), March 6-8, 1994 1994 / p. 14-18: ill

Funktsionaalsete alternatiivsete graafide mudeli süntees digitaallülitustele
Kivi, E.; **Ubar, Raimund-Johannes** XXXII üliõpilaste teaduslik-tehnilise konverentsi ettekannete teesid : pühendatud V. I. Lenini 110. sünniaastapäevale : 16.-18. aprill 1980 1981 / lk. 91 https://www.ester.ee/record=b1322611*est

GA-based test generation for sequential circuits
Brik, Marina; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Ivask, Eero** Proceedings of East–West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 30-34

Gate-level modelling of NBTI-induced delays under process variations
Copetti, Thiago; Cardoso Medeiros, Guilherme; Bolzani Poehls, Leticia; Vargas, Fabian; **Kostin, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 75-80 : ill http://dx.doi.org/10.1109/LATW.2016.7483343

Generating directed tests for C programs using RTL ATPG
Raik, Jaan; Drenkhan, Tiia; **Jenihhin, Maksim**; **Viilukas, Taavi**; **Karputkin, Anton**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings of the IEEE 13th Workshop on RTL and High Level Testing (WRTLT'12) 2012 / p. 1-6

Generation of tests for the localization of single gate design errors in combinational circuits using the stuck-at fault model
Ubar, Raimund-Johannes; Borrione, Dominique XI Brasilian Symposium on Integrated Circuit Design, September 30 - October 3, 1998, Rio de Janeiro, Brazil : proceedings 1998 / p. 51-54 https://ieeexplore.ieee.org/document/715409

Generic interconnect BIST for Network-on-Chip
Jutman, Artur; **Ubar, Raimund-Johannes**; **Raik, Jaan** DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 224-227 : ill

A generic synthesizable NoC switch with a scalable testbench
Govind, Vineeth; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 91-94 : ill

Guest editorial
Lande, Tor Sverre; **Ubar, Raimund-Johannes** Analog integrated circuits and signal processing 1999 / 1, p. 5-6

[H. Bleeker, P.Van Den Eijnden, F.De Jong. Boundary-scan test. Boston : Kluwer Academic, 1993. 225 p. : book review]
Ubar, Raimund-Johannes Engineering applications of artificial intelligence 1994 / p. 86-87 https://www.ester.ee/record=b1200126*est

Handbook of testing electronic systems
Novak, Ondrej; Gramatova, Elena; **Ubar, Raimund-Johannes**; **Jutman, Artur**; **Raik, Jaan** 2005
https://www.ester.ee/record=b2102523*est

Hea teaduse odav väljamüük
Ubar, Raimund-Johannes Postimees 2017 / lk. 6 https://teadus.postimees.ee/4343295/raimund-ubar-hea-teaduse-odav-valjamuuk

A healthier chip?
Ubar, Raimund-Johannes; **Fridolin, Ivo**; **Meigas, Kalju**; **Min, Mart** Public service review : European Union 2010 / p. 132-133 : ill

Hierarchical analysis of short defects between metal lines in CMOS IC
Pleskacz, Witold A.; **Jenihhin, Maksim**; **Raik, Jaan**; Rakowski, Michal; **Ubar, Raimund-Johannes**; Kuzmicz, Wieslaw Proceedings : 11th EUROMICRO Conference on Digital System Design : Architectures, Methods and Tools : (DSD 2008) : September 3-5, 2008, Parma, Italy 2008 / p. 729-734 : ill https://ieeexplore.ieee.org/document/4669309

Hierarchical approach to test generation for digital systems at system, circuit and defect levels
Ubar, Raimund-Johannes 45. Internationales Wissenschaftliches Kolloquium, 04.-06.10.2000 : Tagungsband 2000 / S. 711-716 : Ill

Hierarchical approaches to test generation and fault simulation
Ubar, Raimund-Johannes Radioelectronics and informatics 2003 / p. 204

A hierarchical automatic test pattern generator based on using alternative graphs
Brik, Marina; **Jervan, Gert**; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 4th International Workshop Mixed Design of Integrated Circuits and Systems : MIXDES'97 : Poznan, Poland, 12-14 June 1997 1997 / p. 415-420

Hierarchical calculation of malicious faults for evaluating the fault-tolerance
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan**; **Jervan, Gert**; **Ellervee, Peeter** Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill https://ieeexplore.ieee.org/document/4459544

Hierarchical concurrent test generation for synchronous sequential circuits
Ubar, Raimund-Johannes; **Brik, Marina** Proceedings of the 7th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2000 : Gdynia, Poland, 15-17 June 2000 2000 / p. 533-538 : ill

Hierarchical defect level test quality analysis
Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** VILAB User Forum 2000 / [11] p

Hierarchical defect-oriented fault simulation for digital circuits
Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** IEEE European Test Workshop 2000 / p. 151-156 https://ieeexplore.ieee.org/document/873781

Hierarchical defect-oriented fault simulation for digital circuits
Blyzniuk, M.; Cibakova, Tatiana; Gramatova, Elena; Kuzmicz, W.; Lobur, M.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** IEEE European Test Workshop : 23-26 May 2000, Cascais, Portugal : ETW 2000 : proceedings 2000 / p. 69-74 : ill https://ieeexplore.ieee.org/document/873781

Hierarchical design error diagnosis in combinational circuits by stuck-at fault test patterns
Ubar, Raimund-Johannes; **Jutman, Artur** Proceedings of the 6th International Conference on Mixed Design of Integrated Circuits and Systems : MIXDES'99 : Krakow, Poland, 17-19 June 1999 1999 / p. 437-442 : ill https://www.sciencedirect.com/science/article/pii/S0026271499002036

Hierarchical fault diagnosis in embedded digital systems with multi-level decision diagrams [Electronic resource]
Ubar, Raimund-Johannes; **Evartson, Teet**; **Lensen, Harri**; **Aarna, Margit** 5th International Conference on Industrial Automation = Cinquieme Conference Internationale sur l'Automatisation Industrielle : June 11-13, 2007, Montreal, Canada 2007 / [6] p. [CD-ROM]

Hierarchical fault simulation for finite state machines
Brik, Marina; **Raik, Jaan**; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 145-148 : ill

Hierarchical fault simulation in digital systems
Ubar, Raimund-Johannes; **Raik, Jaan**; **Ivask, Eero**; **Brik, Marina** International Symposium on Signals, Circuits and Systems : SCS 2001 : July 10-11, 2001, Iasi, Romania : proceedings 2001 / p. 181-184 : ill

Hierarchical identification of NBTI-critical gates in nanoscale logic
Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Hierarchical identification of untestable faults in sequential circuits

Raik, Jaan; **Ubar, Raimund-Johannes**; **Krivenko, Anna**; **Kruus, Margus** 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 668-671 : ill
http://dx.doi.org/10.1109/DSD.2007.4341539

Hierarchical physical defect reasoning in digital circuits
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Brik, Marina** Estonian journal of engineering 2011 / 3, p. 185-200

Hierarchical test generation based on alternative graph model
Ubar, Raimund-Johannes Proceedings of the Second Workshop on Hierarchical Test Generation : Microelectronics Technology Park, Duisburg, Germany, September 25-26, 1995 1995 / p. 18

Hierarchical test generation for combinational circuits with real defects coverage
Cibakova, Tatiana; Fischerova, Maria; Gramatova, Elena; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** Microelectronics reliability 2002 / p. 1141-1149 : ill https://www.sciencedirect.com/science/article/pii/S002627140200080X

Hierarchical test generation for complex digital systems with control and data processing parts
Ubar, Raimund-Johannes; **Raik, Jaan** "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 43-52

Hierarchical test generation for digital circuits represented by Decision Diagrams : thesis on informatics and system engineering
Raik, Jaan 2001 https://www.ester.ee/record=b1578107*est

Hierarchical test generation for digital systems
Brik, Marina; **Jervan, Gert**; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Mixed design of integrated circuits and systems 1998 / p. 131-136: ill https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_20

Hierarchical test generation for digital systems based on combining bottom-up and top-down approaches
Raik, Jaan; **Ubar, Raimund-Johannes** World Multiconference on Systemics, Cybernetics and Informatics, July 12-16, 1998, Orlando, Florida : proceedings. Vol. 1 1998 / p. 374-381: ill

Hierarchical test generation for finite state machines
Brik, Marina; **Ubar, Raimund-Johannes** BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 1 1994 / p. 319-324: ill

Hierarchical test generation with multi-level decision diagram models
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 7th IEEE North Atlantic Test Workshop, West Greenwich RI, USA, May 28-29, 1998 1998 / p. 26-33
https://www.academia.edu/67811738/Hierarchical_Test_Generation_with_Multi_Level_Decision_Diagram_Models?hb-g-sw=7883185

Hierarchical test generation. SEMI show slides
Ubar, Raimund-Johannes; **Raik, Jaan** "Test, Assembly and Packaging" : SEMICON Technical Symposium : Singapur, May 3-6, 1999 1999 / p. 53-64

Hierarchical test synthesis for digital systems using alternative graph model
Ubar, Raimund-Johannes Quantitative aspects of designing and validating dependable computing systems 1995

Hierarchical timing-critical paths analysis in sequential circuits
Jürimägi, Lembit; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan**; **Devadze, Sergei**; **Kostin, Sergei** 2018 IEEE 28th International Symposium on Power and Timing Modeling, Optimization and Simulation (PATMOS 2018) : 2 – 4 July 2018, Spain 2018 / 6 p. : ill https://doi.org/10.1109/PATMOS.2018.8464176

High level fault modeling in digital systems
Ubar, Raimund-Johannes; **Aarna, Margit**; **Brik, Marina**; **Raik, Jaan** Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 486-491

High quality test generation for digital systems
Ubar, Raimund-Johannes; **Aarna, Margit**; **Kruus, Helena**; **Raik, Jaan** Romanian journal of information science and technology 2005 / 1, p. 73-84 : ill

High-level combined deterministic and pseudo-exhuastive test generation for RISC processors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Gürsoy, Cemil Cem**; **Raik, Jaan** 2019 IEEE European Test Symposium (ETS) : proceedings 2019 / 6 p. : ill https://doi.org/10.1109/ETS.2019.8791526

High-Level Combined Deterministic and Pseudo-exhuastive Test Generation for RISC Processors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** 2019 IEEE European Test Symposium

(ETS) : ETS 2019, May 27-31, 2019, Baden-Baden, Germany : Proceedings 2019 / 6 p. : ill https://doi.org/10.1109/ETS.2019.8791526

High-level decision diagram based fault models for targeting FSMs
Raik, Jaan; **Ubar, Raimund-Johannes**; **Viilukas, Taavi** 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 353-358 : ill http://dx.doi.org/10.1109/DSD.2006.60

High-Level Decision Diagram manipulations for code coverage analysis
Minakova, Karina; **Reinsalu, Uljana**; **Tšepurov, Anton**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; **Ellervee, Peeter** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level decision diagrams based coverage metrics for verification and test
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Reinsalu, Uljana**; **Ubar, Raimund-Johannes** LATW 2009 : 10th IEEE Latin American Test Workshop : Buzios, Rio de Janero, Brazil, March 2-5, 2009 2009 / [6] p. : ill http://dx.doi.org/10.1109/LATW.2009.4813792

High-level decision diagrams for improving simulation performance of digital systems
Ubar, Raimund-Johannes; **Raik, Jaan**; Morawiec, Adam SCI 2000 : World Multiconference on Systemics, Cybernetics and Informatics : July 23-26, 2000, Orlando, Florida, USA : proceedings. Volume IX, Industrial Systems 2000 / p. 62-67 : ill https://hal.science/hal-01396447v1

High-level design error diagnosis using backtrace on decision diagrams
Raik, Jaan; **Repinski, Urmas**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Tšepurov, Anton** 28th Norchip Conference : Tampere, Finland, 15-16 November 2010 : conference program and papers 2010 / [4] p. : ill http://dx.doi.org/10.1109/NORCHIP.2010.5669486

High-level fault diagnosis in RISC processors with Implementation-Independent Functional Test
Oyeniran, Adeboye Stephen; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** 2022 IEEE Computer Society Annual Symposium on VLSI (ISVLSI) : Nicosia, Cyprus : 04-06 July 2022 2022 / p. 32-37 https://doi.org/10.1109/ISVLSI54635.2022.00019

High-level functional test generation for microprocessor modules
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes** Proceedings of 26th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2019 : Rzeszów, Poland, June 27 - 29, 2019 2019 / p. 356-361 : ill https://doi.org/10.23919/MIXDES.2019.8787131

High-Level Implementation-Independent Functional Software-Based Self-Test for RISC Processors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** Journal of electronic testing : theory and applications 2020 / p. 87-103 https://doi.org/10.1007/s10836-020-05856-7

High-level implementation-independent software-based self-test for RISC type microprocessors = Mikroprotsessorite tarkvarapõhine implementatsioonist mittesõltuv funktsionaalne enesekontroll
Oyeniran, Adeboye Stephen 2020 https://digikogu.taltech.ee/et/Item/08a75fbb-3f71-4fe4-b3d0-3f37a9a5f36d

High-level modeling and testing of multiple control faults in digital systems
Jasnetski, Artjom; **Oyeniran, Adeboye Stephen**; **Tšertov, Anton**; Schölzel, Mario; **Ubar, Raimund-Johannes** Formal proceedings of the 2016 IEEE 19th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 20-22, 2016, Košice, Slovakia 2016 / [6] p. : ill http://dx.doi.org/10.1109/DDECS.2016.7482445

High-level path activation technique to speed up sequential circuit test generation
Raik, Jaan; **Ubar, Raimund-Johannes** European Test Workshop 1999 : proceedings, May 25-28, 1999, Constance, Germany 1999 / p. 84-89 : ill https://ieeexplore.ieee.org/document/804289

High-level synthesis and test in the MOSCITO-based virtual laboratory
Schneider, Andre; Diener, Karl-Heinz; **Jervan, Gert**; Peng, Z.; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Hollstein, Thomas; Glesner, M. BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 287-290 : ill

High-level test data generation for software based self-test in microprocessors
Oyeniran, Adeboye Stephen; **Jasnetski, Artjom**; **Tšertov, Anton**; **Ubar, Raimund-Johannes** 2017 6th Mediterranean Conference on Embedded Computing (MECO) : including ECYPS'2017 : proceedings : research monograph : Bar, Montenegro, June 11th-15th, 2017 2017 / p. 86-91 : ill https://doi.org/10.1109/MECO.2017.7977167

High-level test generation for processing elements in many-core systems
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Azad, Siavoosh Payandeh**; **Raik, Jaan** 12th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC2017), July 12-14, 2017, Madrid, Spain : proceedings 2017 / 8 p. : ill http://dx.doi.org/10.1109/ReCoSoC.2017.8016156

High-level test synthesis with hierarchical test generation
Jervan, Gert; Eles, Petru; Peng, Zebo; **Raik, Jaan**; **Ubar, Raimund-Johannes** 17th NORCHIP Conference : Oslo, Norway, 8-9 November 1999 : proceedings 1999 / p. 291-296

High-speed logic level fault simulation
Ubar, Raimund-Johannes; **Devadze, Sergei** Design and test technology for dependable systems-on-chip 2011 / p. 310-335 : ill
https://www.igi-global.com/chapter/high-speed-logic-level-fault/51407

How to generate high quality tests for digital systems
Ubar, Raimund-Johannes; **Aarna, Margit**; **Kruus, Helena**; **Raik, Jaan** 2004 International Semiconductor Conference : 27th edition, October 4-6, 2004, Sinaia, Romania : CAS 2004 proceedings. Volume 2 2004 / p. 459-462 : ill
http://dx.doi.org/10.1109/SMICND.2004.1403048

How to prove that a circuit is fault-free?
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings : 15th Euromicro Conference on Digital System Design DSD 2012 : 5-8 September 2012, Cesme, Izmir, Turkey 2012 / p. 427-430 : ill
https://www.researchgate.net/publication/262271409_How_to_Prove_that_a_Circuit_is_Fault-Free

A hybrid BIST architecture and its optimization for SoC testing
Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes**; **Kruus, Helena** Proceedings of the 3rd International Symposium on Quality Electronic Design : ISQED 2002, March 18-21, 2002, San Jose, California 2002 / p. 273-279 : ill
https://ieeexplore.ieee.org/document/996750

Hybrid BIST energy minimisation technique for system-on-chip testing
Jervan, Gert; **Peng, Zebo**; **Shchenova, Tatjana**; Ubar, Raimund-Johannes IEE proceedings computers & digital techniques 2006 / 4, p. 208-216 : ill https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=5ae755d323ccba87f8ff886334e3dd6d33560874

Hybrid BIST methodology for testing core-based systems
Jervan, Gert; **Ubar, Raimund-Johannes**; Peng, Zebo Proceedings of the Estonian Academy of Sciences. Engineering 2006 / 3-2, p. 300-322 : ill

Hybrid BIST optimization for core-based systems with test pattern broadcasting
Ubar, Raimund-Johannes; **Jenihhin, Maksim**; **Jervan, Gert**; Peng, Zebo DELTA 2004 : second IEEE International Workshop on Electronic Design, Test and Applications : 28-30 January 2004, Perth, Australia : proceedings 2004 / p. 3-8 : ill
https://ieeexplore.ieee.org/document/1409808

Hybrid BIST optimization using reseeding and test set compaction
Jervan, Gert; **Orasson, Elmet**; **Kruus, Helena**; **Ubar, Raimund-Johannes** 10th Euromicro Conference on Digital System Design Architectures, Methods and Tools, DSD 2007 : 29-31 August 2007, Lübeck, Germany : proceedings 2007 / p. 596-603 : ill
http://dx.doi.org/10.1109/DSD.2007.4341529

Hybrid BIST optimization using reseeding and test set compaction
Jervan, Gert; **Orasson, Elmet**; **Kruus, Helena**; **Ubar, Raimund-Johannes** Microprocessors and microsystems 2008 / 5/6, p. 254-262 : ill https://www.sciencedirect.com/science/article/abs/pii/S0141933108000288

Hybrid BIST scheduling for NoC-based SoCs
Jervan, Gert; **Shchenova, Tatjana**; **Ubar, Raimund-Johannes** Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 141-144 : ill https://ieeexplore.ieee.org/document/4126966

Hybrid BIST time minimization for core-based systems with STUMPS architecture
Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 3-5 November 2003, Boston, Massachusetts : proceedings 2003 / p. 225-232 : ill
https://ieeexplore.ieee.org/document/1250116

Hybrid built-in self-test : methods and tools for analysis and optimization of BIST = Sisseehitatud hübriidne isetestimine : meetodid ja vahendid analüüsiks ning optimeerimiseks
Orasson, Elmet 2007 https://www.ester.ee/record=b2305436*est

Hybrid functional BIST for digital systems
Mazurova, Natalja; **Smahtina, Julia**; **Ubar, Raimund-Johannes** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 205-208 : ill

HyFBIST : hybrid functional built-in self-test in microprogrammed data-paths of digital systems
Ubar, Raimund-Johannes; Mazurova, Natalja; Smahtina, Julia; **Orasson, Elmet**; **Raik, Jaan** Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 497-502 : ill

"Ideat ovat pääomaamme" : [Raimund Ubar]
Ubar, Raimund-Johannes Net 1992 / s. 20 : kuva

Identification and rejuvenation of NBTI-critical logic paths in nanoscale circuits
Jenihhin, Maksim; Squillero, Giovanni; **Tihhomirov, Valentin**; **Kostin, Sergei**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications (JETTA) 2016 / p. 273-289 : ill https://doi.org/10.1007/s10836-016-5589-x Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Identifying NBTI-critical paths in nanoscale logic
Ubar, Raimund-Johannes; Vargas, Fabian; **Jenihhin, Maksim**; **Raik, Jaan**; **Kostin, Sergei**; Bolzani Poehls, Leticia 16th Euromicro Conference series on Digital System Design : DSD 2013 : proceedings : 4-6 September 2013, Santander, Spain 2013 / p. 136-141 : ill

Identifying untestable faults in sequential circuits using test path constraints
Viilukas, Taavi; **Karputkin, Anton**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill https://link.springer.com/article/10.1007/s10836-012-5312-5

Implementation-independent functional test for transition delay faults in microprocessors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / p. 646-650 https://doi.org/10.1109/DSD51259.2020.00105

Implementation-independent functional test generation for RISC microprocessors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** VLSI-SoC 2019 : 27th IFIP/IEEE International Conference on Very Large Scale Integration : [proceedings] 2019 / p. 82-87 : ill https://doi.org/10.1109/VLSI-SoC.2019.8920323

Implementation-independent test generation for a large class of faults in RISC processor modules
Jenihhin, Maksim; **Oyeniran, Adeboye Stephen**; **Raik, Jaan**; **Ubar, Raimund-Johannes** 24th Euromicro Conference on Digital System Design (DSD) 2021 https://doi.org/10.1109/DSD53832.2021.00090

An improved estimation methodology for hybrid BIST cost calculation
Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes**; Korelina, Olga Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 297-300 : ill https://ieeexplore.ieee.org/document/1423882

An improved estimation technique for hybrid BIST test set generation
Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes**; Korelina, Olga DDECS : 8th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems : April 13-16, 2005, Sopron, Hungary : proceedings 2005 / p. 182-185 : ill https://www.ida.liu.se/labs/eslab/publications/pap/db/ddecs05.pdf

Improved fault emulation for synchronous sequential circuits
Raik, Jaan; **Ellervee, Peeter**; **Tihhomirov, Valentin**; **Ubar, Raimund-Johannes** Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

An improved test generation approach for sequential circuits using decision diagrams
Brik, Marina; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 155-158: ill

Improved testability calculation for digital circuits
Ubar, Raimund-Johannes; Heinlaid, J.; Raun, L. 19th NORCHIP Conference, Kista, Sweden, 12-13 November 2001 : proceedings 2001 / p. 264-270 : ill

Improving the efficiency of timing simulation in digital circuits by using structurally synthesized BDDs
Ubar, Raimund-Johannes; **Jutman, Artur**; Peng, Z. IEEE Norchip Conference 2000 / p. 254-261

Increasing the speed of delay simulation in digital circuits
Ubar, Raimund-Johannes; **Jutman, Artur** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 31-34 : ill

Infotehnoloogia teaduskond
Gordon, Boris; **Velmre, Enn**; **Einer, Lauri**; **Tamm, Uljas**; **Meister, Ants**; **Korsen, Viljo**; **Märtens, Olev**; **Parve, Toomas**; **Ubar, Raimund-Johannes**; **Min, Mart** Leiutajaid ja leiutisi Tallinna Tehnikaülikoolis 1922-2007 2008 / lk. 34-47 : ill https://www.ester.ee/record=b2412718*est

Innovatsiooni võimalikkusest Eestis
Ubar, Raimund-Johannes Postimees 1998 / 9. apr., lk. 9

Insener projekteerib usaldust : [ka TTÜ arvutitehnika instituudi töödest]
Ubar, Raimund-Johannes Arvutimaailm 2011 / 7/8, lk. 8-9 : ill https://artiklid.elnet.ee/record=b2423013*est

Inseneri ja tehnoloogia võidujooksust nanomeeterdistantsil, ehk, Tehnoloogia valitsemisest ja usaldamisest : akadeemiline ettekanne 10. novembril 2010 Eesti Teaduste Akadeemias
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2010 2011 / lk. 249-260

Inseneride ärkamisaeg
Ubar, Raimund-Johannes Postimees 2011 / lk. 10

Inseneriharidus mikroelektroonika ajastul
Ubar, Raimund-Johannes Tehnikaülikool 1998 / 16. nov., lk. 6

Integrated design and test generation under Internet based environment MOSCITO
Schneider, Andre; **Ivask, Eero**; **Ubar, Raimund-Johannes** Euromicro Symposium on Digital System Design : Architectures, Methods and Tools : September 4-6, 2002, Dortmund, Germany : proceedings 2002 / p. 187-194 : ill
http://dx.doi.org/10.1109/DSD.2002.1115368

Integration of digital test tools to the internet-based environment MOSCITO
Schneider, Andre; Diener, Karl-Heinz; Elst, Günter; **Ivask, Eero**; **Raik, Jaan**; **Ubar, Raimund-Johannes** SCI 2003 : the 7th World Multiconference on Systemics, Cybernetics and Informatics : July 27-30, 2003, Orlando, Florida, USA : proceedings. Volume VIII, Applications of Informatics and Cybernetics in Science and Engineering 2003 / p. 136-141 : ill
https://www.researchgate.net/publication/250063424_Integration_of_Digital_Test_Tools_to_the_Internet-Based_Environment_MOSCITO

Integreeritud elektroonikasüsteemide ja biomeditsiinitehnika tippkeskus
Ubar, Raimund-Johannes Eesti Päevaleht 2012 / Eesti teaduse tippkeskused, lk. 3

Integreeritud elektroonikasüsteemide ja biomeditsiinitehnika tippkeskus CEBE
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2010 2011 / lk. 29-40

Interactive presentation abstract : automated correction of design errors by edge redirection on high-level decision diagrams [Electronic resource]
Karputkin, Anton; **Ubar, Raimund-Johannes**; **Tombak, Mati**; **Raik, Jaan** IEEE International High Level Design Validation and Test Workshop (HLDVT'11), November 9-11, 2011, Napa Valley, CA 2011 / p. 83 : ill. [CD-ROM]
http://doi.ieeecomputersociety.org/10.1109/HLDVT.2011.6113980

Interactive teaching software "Introduction to digital test"
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich; **Orasson, Elmet** 45. Internationales Wissenschaftliches Kolloquium, 04.-06.10.2000 : Tagungsband 2000 / S. 949-954

Internet based test generation and fault simulation
Ivask, Eero; **Ubar, Raimund-Johannes**; **Raik, Jaan**; Schneider, Andre IEEE Design and Diagnostics of Electronic Circuits and Systems - IEEE DDECS 2001 : Fourth International Workshop on IEEE Design and Diagnostics of Electronic Circuits and Systems : Györ, Hungary, April 18-20, 2001 2001 / p. 57-60 : ill

Internet-based collaborative test generation with MOSCITO [Electronic resource]
Schneider, Andre; **Ivask, Eero**; Miklos, P.; **Raik, Jaan**; Diener, Karl-Heinz; **Ubar, Raimund-Johannes**; Cibakova, Tatiana; Gramatova, Elena SIGDA publications on CD-ROM : DATE'02 : Design, Automation and Test in Europe, Paris, France, March 4-8, 2002 2002 / [6] p. [CD-ROM] https://www.cecs.uci.edu/~papers/date07/PAPERS/2002/DATE02/PDFFILES/02E_2.PDF

Internet-based software for teaching test of digital circuits
Ubar, Raimund-Johannes; **Orasson, Elmet**; Wuttke, Heinz-Dietrich 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 659-662 : ill https://ieeexplore.ieee.org/document/1003344

Internet-based software for teaching test of digital circuits
Ubar, Raimund-Johannes; **Jutman, Artur**; **Orasson, Elmet**; **Raik, Jaan**; **Evartson, Teet**; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 4th European Workshop on Microelectronics Education : EWME 2002, Spain, May 23-24, 2002 2002 / p. 317-320 : ill https://ieeexplore.ieee.org/document/1003344

Internet-based testability-driven test generation in the virtual environment MOSCITO
Schneider, Andre; Diener, Karl-Heinz; Elst, G.; **Ivask, Eero**; **Raik, Jaan**; **Ubar, Raimund-Johannes** International Federation for Information Processing IFIP : International Workshop on IP-Based SoC Design 2002 : proceedings : Grenoble, October 30-31, 2002 2002 / p. 357-362 : ill http://publica.fraunhofer.de/dokumente/N-287433.html

Investigating defects in digital circuits by Boolean differential equations

Kruus, Helena; **Orasson, Elmet**; **Robal, Tarmo**; **Ubar, Raimund-Johannes** The 4th International Conference "Distance Learning - Educational Sphere of XXI Century" (DLESC'04) 2004 / p. 432-435

Investigation and development of test generation methods for control part of digital systems
Brik, Marina 2002 http://www.ester.ee/record=b1688656*est

Investigations of the diagnosibility of digital networks with BIST
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** 10th IEEE Latin American Test Workshop : 2-5 March 2009, Brazil 2009 / [6] p. : ill

IST project REASON : handbook of testing electronic systems
Novak, Ondrej; Gramatova, Elena; **Ubar, Raimund-Johannes** IEEE Proceedings of the 5th European Dependable Computing Conference : EDCC-5 : Budapest, 2005 2005 / p. 15-18

An iterative approach to test time minimization for parallel hybrid BIST architecture
Ubar, Raimund-Johannes; **Jenihhin, Maksim**; **Jervan, Gert**; Peng, Z. 5th IEEE Latin-American Test Workshop - LATW 2004 : Cartagena, Colombia, 2004 : digest of papers 2004 / p. 98-103 : ill https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf

An iterative approach to test time minimization for parallel hybrid BIST architectures
Ubar, Raimund-Johannes; **Jenihhin, Maksim**; **Jervan, Gert**; Peng, Z. System-on-Chip Conference 2004 : Bastad, Sweden 2004 / p. ? https://www.ida.liu.se/labs/eslab/publications/pap/db/latw04.pdf

Java applet for self-learning of digital test issues [Electronic resource]
Ubar, Raimund-Johannes; **Orasson, Elmet**; **Evartson, Teet** 13th EAEEIE Annual Conference, 8th-10th April, 2002, York, England 2002 / [4] p. [CD-ROM]

Java applets support for an asynchronous-mode learning of digital design and test
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich ITHET 2003 proceedings : 4th International Conference on Information Technology Based Higher Education and Training : July 7-9, 2003, Marrakech, Morocco 2003 / p. 397-401 : ill https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=92f0b0e5011a2192d5a1b98baa751cb8cd2f7ff3

Java technology based training system for teaching digital design and test
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 283-286 : ill

Jooksujalu : [intervjuu Raimund-Johannes Ubariga]
Ubar, Raimund-Johannes Põline partituur : intervjuud akadeemikutega 2011 / lk. 81-104 : portr

Jänestena tsivilisatsiooni hüvede trammis
Ubar, Raimund-Johannes Rahva Hääl 1994 / 7. nov.: ill https://artiklid.elnet.ee/record=b1887219*est

Järgmine sajand on teadlase nägu : [arvamust avaldavad Jüri Engelbrecht, Raimund Ubar jt.]
Hansen, Regina; **Engelbrecht, Jüri**; **Ubar, Raimund-Johannes** Eesti Päevaleht 1999 / 18. dets., lk. 18 : fot

20 aastat maailma testiteaduse tippkonkurentsis
Ubar, Raimund-Johannes Mente et Manu 2015 / lk. 12-13 : fot https://artiklid.elnet.ee/record=b2749536*est

Kas Eesti kultuuri päästaks üksainus universitas? ehk Teaduse ja hariduse väärtustamisest Eestis
Ubar, Raimund-Johannes Postimees 1994 / 21. nov

Kas Eestil on vaja oma mikroelektroonikat?
Ubar, Raimund-Johannes Arvutimaailm 1993 / 2, lk. 46-47

Kas oleme õigel teel?
Ubar, Raimund-Johannes Sirp 2016 / lk. 10-11 https://www.sirp.ee/s1-artiklid/c21-teadus/kas-oleme-oigel-teel/

Kas Tehnikaülikoolis võiks olla mitu arvutuskeskust ehk mis saab elektroonika kompetentsuskeskusest?
Ubar, Raimund-Johannes; **Küttner, Rein** Tehnikaülikool 1996 / 18. dets., lk. 3-6: ill https://www.ester.ee/record=b5309277*est

Keerukate arvutisüsteemide uurimine Tallinna Tehnikaülikoolis
Jervan, Gert; **Ellervee, Peeter**; **Ubar, Raimund-Johannes** Tallinna Tehnikaülikooli aastaraamat 2007 2008 / lk. 42-60 : ill

Kes on teaduste doktor?
Ubar, Raimund-Johannes Tehnikaülikool 1993 / 28. jaan., lk. 1-3 https://www.ester.ee/record=b5309277*est

Kes vastutab Eesti teaduse eest?
Ubar, Raimund-Johannes Postimees 1997 / 19. dets., lk. 9

Kes vastutab Eesti teaduse eest?
Ubar, Raimund-Johannes Tallinna Ülikoolid 1998 / 1, lk. 8-9

Kihiline kõrgharidus
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2000 2001 / lk. 281-284. (Insener ja inseneriharidus)

Kihiline kõrgharidus : riigiülikoolide reformimisel tuleks õppida eraülikoolide kogemustest
Ubar, Raimund-Johannes Luup 2000 / 7, lk. 18-20 https://artiklid.elnet.ee/record=b2334789*est

"Kihilisest" kõrgharidusest ehk õppemaksust ja ülikoolide finantseerimisest
Ubar, Raimund-Johannes Tehnikaülikool 2000 / 3. apr., lk. 2-3

Kolm akadeemikut - ühe rühma poisid : [vestlus Olav Aarna, Leo Mõtuse ja Raimund-Johannes Ubariga]
Aarna, Olav; **Mõtus, Leo**; **Ubar, Raimund-Johannes** Horisont 2001 / lk. 4-9 : fot https://www.ester.ee/record=b1072243*est http://www.digar.ee/id/nlib-digar:292222

Kolm akadeemikut - ühe rühma poisid : [vestlusringis Leo Mõtus, Olav Aarna ja Raimund Ubar]
Mõtus, Leo; **Aarna, Olav**; **Ubar, Raimund-Johannes** Põline partituur : Eesti teadlased horisondil 2007 / lk. 142-150 : fot https://www.ester.ee/record=b2235601*es

Kolm tiiru ümber heinakuhja? : [loengupidamisest ja õpetamisest]
Ubar, Raimund-Johannes Õpetajate Leht 2011 / lk. 7 https://artiklid.elnet.ee/record=b2409366*est

Kordsete rikete diagnostika järjestiklülitustes
Puulinn, S.; **Ubar, Raimund-Johannes** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 43 https://www.ester.ee/record=b2449987*est

Korvitäis mõtteid teadusmetsast
Ubar, Raimund-Johannes Akadeemia 2022 / lk. 540-546 https://www.ester.ee/record=b1071914*est

Kuidas fookustada korraga kaugele ja lähedale, ehk, Kuidas ülikool saaks paremini teenida ühiskonda
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2009 2010 / lk. 13-15 https://www.ester.ee/record=b1212786*est

Kuidas grupp Tehnikaülikooli tudengeid Prantsusmaal elektroonikat õppimas käis
Koort, Marko; **Ubar, Raimund-Johannes** Tehnikaülikool 1996 / 3. apr., lk. 4-5; 30. apr., lk. 5-8; 23. mai, lk. 4-6; 14. juuni, lk. 4-7 https://www.ester.ee/record=b5309277*est

Kuidas ülikool saaks paremini ühiskonda teenida
Ubar, Raimund-Johannes Postimees 2010 / 16. märts, lk. 13 https://leht.postimees.ee/237399/raimund-ubar-kuidas-ulikool-saaks-paremini-uhiskonda-teenida

Kultuuri funktsioon on resistance
Ubar, Raimund-Johannes Sirp 1993 / 8. okt., lk. 3: portr https://artiklid.elnet.ee/record=b1911203*est

Kõrgema tehnilise hariduse ja tehnilise mõtte areng Eestis
Kulbach, Valdek; **Hinrikus, Hiie**; **Järvik, Jaan**; **Kanasaar, Eduard**; **Kilk, Aleksander**; **Metusala, Tiit**; **Mägi, Vahur**; **Tamm, Uljas**; **Tapupere, Olev**; **Tiismus, Hugo**; **Ubar, Raimund-Johannes**; **Velmre, Enn** 1988 https://www.ester.ee/record=b1243393*est

Kõrgharidus mitme tule all
Ubar, Raimund-Johannes Mente et Manu 2010 / lk. 5 : fot https://www.ester.ee/record=b1242496*est

Kõrgharidus on võime näha puude taga metsa : [kõne TTÜ 90. aastapäeva aktusel 17. septembril 2008 TTÜ aulas]
Ubar, Raimund-Johannes Tallinna Tehnikaülikool 90 : [artiklikogumik] 2009 / lk. 50-55

Kõrgharidus on võime näha puude taga metsa : [kõne TTÜ 90. aastapäeva pidulikul koosolekul 17. sept. 2008 TTÜ aulas]
Ubar, Raimund-Johannes Mente et Manu 2008 / 26. sept., lk. 3 : fot https://www.ester.ee/record=b1242496*est

Laboratory course for training "Digital design and test"
Ubar, Raimund-Johannes; **Tulit, Viljar**; Buldas, Ahto; **Saarepera, Märt** Fourth EUROCHIP Workshop on VLSI Design Training, 29 September to 1 October 1993, Toledo : [proceedings] 1993 / p. 112-117: ill

Laboratory framework TEAM for investigating the dependability issues of microprocessor systems

Jasnetski, Artjom; **Tšertov, Anton**; **Ubar, Raimund-Johannes**; **Kruus, Helena** 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 80-83 : ill

Laboratory training for teaching design and test of digital circuits
Jutman, Artur; **Ubar, Raimund-Johannes** Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 521-524 : ill https://pld.ttu.ee/~artur/papers/TestLabs-MIXDES01.pdf

Lapik maa ja eestlased : Euroopa esinduskonverentsil DATE'99 [Design Automation and Test in Europe] Münchenis
Ubar, Raimund-Johannes Tehnikaülikool 1999 / 5. apr., lk. 4 https://www.ester.ee/record=b5309277*est

Layout to logic defect analysis for hierarchical test generation
Jenihhin, Maksim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Pleskacz, Witold A.; Rakowski, Michal Proceedings of the 2007 IEEE Workshop on Design and Diagnostic Circuits and Systems : April 11-13, 2007, Krakow, Poland 2007 / p. 35-40 : ill http://dx.doi.org/10.1109/DDECS.2007.4295251

Learning digital test and diagnostics via internet
Ubar, Raimund-Johannes; **Jutman, Artur**; **Kruus, Margus**; **Orasson, Elmet**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International journal of online engineering 2007 / 1, [9] p. : ill https://www.db-thueringen.de/servlets/MCRFileNodeServlet/dbt_derivate_00032681/iJOE_1681-1221_03_2007_1_361.pdf

Learning digital test and diagnostics via internet [Electronic resource]
Ubar, Raimund-Johannes; **Jutman, Artur**; **Kruus, Margus**; **Orasson, Elmet**; **Devadze, Sergei**; Wuttke, Heinz-Dietrich International journal of computing & information sciences 2006 / 2, p. 86-96 : ill

LFSR polynomial and seed selection using genetic algorithm
Aleksejev, E.; **Jutman, Artur**; **Ubar, Raimund-Johannes** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 179-182 : ill

Linear algorithms for recognizing and parsing superpositional graphs
Peder, Ahti; Nestra, Härmel; **Raik, Jaan**; **Tombak, Mati**; **Ubar, Raimund-Johannes** Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 325-339 : ill http://dx.doi.org/10.2298/FUEE1103325P

Linear algorithms for testing superpositional graphs
Peder, Ahti; Nestra, Härmel; **Raik, Jaan**; **Tombak, Mati**; **Ubar, Raimund-Johannes** Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 111-118 : ill

Localization of single-gate design errors in combinational circuits by diagnostic information about stuck-at faults
Ubar, Raimund-Johannes; Borrione, Dominique Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 73-79 https://www.researchgate.net/publication/238687832_Localization_of_Single_Gate_Design_Errors_in_Combinational_Circuits_by_Diagnostic_Information_about_Stuck-at_Faults

Logic simulation and fault collapsing with shared structurally synthesized BDDs
Mironov, Dmitri; **Ubar, Raimund-Johannes**; **Raik, Jaan** 2014 19th IEEE European Test Symposium (ETS) : May 26th-30th, 2014, Paderborn, Germany : proceedings 2014 / [2] p. : ill

Low-cost CAD software for teaching digital test
Ubar, Raimund-Johannes; **Raik, Jaan**; **Paomets, Priidu** First European Workshop on Microelectronics Education, Villard de Lans, France, February 5-6, 1996 : proceedings 1996 / p. 48

Low-cost CAD system for teaching digital test
Ubar, Raimund-Johannes; **Raik, Jaan**; **Paomets, Priidu**; **Ivask, Eero**; **Jervan, Gert**; **Markus, Antti** Microelectronics education : proceedings of the European Workshop, Grenoble, France, 5-6 Feb 1996 1996 / p. 185-188

Lower bounds of the size of shared structurally synthesized BDDs
Ubar, Raimund-Johannes; **Mironov, Dmitri** Proceedings of the 2014 IEEE 17th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 23-25, 2014, Warsaw, Poland 2014 / p. 77-82 : ill

Lühinägelik rahastamislahendus
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2002 2003 / lk. 125-127

Lühinägelik rahastamislahendus : [Eesti valitsus võtmas suunda projektipõhisele investeerimisele]
Ubar, Raimund-Johannes Postimees 2002 / 17. mai, lk. 11 https://arvamus.postimees.ee/1939989/luhinagelik-rahastamislahendus

Macro level defect-oriented diagnosability of digital circuits
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 149-152 : ill

Macro level defect-oriented diagnosability of digital circuits
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 53-56 : ill

Mapping faults in hierarchical testing of digital systems
Ubar, Raimund-Johannes International Conference on Computer, Communication and Control Technologies CCCT'03 and the 9th International Conference on Information Systems, Analysis and Synthesis ISAS'03 : July 31 - August 1-2, Orlando, Florida, USA : proceedings. Volume I, Computing/Information Systems and Technologies 2003 / p. 14-19 : ill

Mapping physical defects to logic level for defect oriented testing
Ubar, Raimund-Johannes SCS 2003 : International Symposium on Signals, Circuits and Systems : July 10-11, 2003, Iasi, Romania : proceedings. Vol. 2 2003 / p. 453-456 : ill https://ieeexplore.ieee.org/document/5731320

Measuring and identifying aging-critical paths in FPGAs
Pfeifer, Petr; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; Pliva, Zdenek MEDIAN 2015 : the 4th Workshop on Manufacturable and Dependable Multicore Architectures at Nanoscale : March 13, 2015, Grenoble, France 2015 / p. 56-61 : ill

A method for crosstalk fault detection in on-chip buses
Bengtsson, Tomas; **Jutman, Artur**; **Ubar, Raimund-Johannes**; Kumar, Shashi Norchip : proceedings : Oulu, Finland, 21-22 November 2005 2005 / p. 285-288 : ill https://doi.org/10.1109/NORCHP.2005.1597045

Method for testing the brain
Hinrikus, Hiie; **Bachmann, Maie**; **Lass, Jaanus**; **Tuulik, Viiu**; **Ubar, Raimund-Johannes** 5th European Conference of the International Federation for Medical and Biological Engineering : 14-18 September 2011, Budapest, Hungary 2012 / p. 1198-1201 : ill

Methods for improving the accuracy and efficiency of fault simulation in digital systems = Meetodid digitaalsüsteemide rikete simuleerimise täpsuse ja efektiivsuse tõstmiseks
Kõusaar, Jaak 2019 https://digi.lib.ttu.ee/i/?11667

Methods for improving the performance of simulation
Mermet, J.; Morawiec, A.; **Ubar, Raimund-Johannes** Annual report 2000 / TIMA Laboratory 2001 / p. 90-94

Methods for improving the simulation performance
Mermet, J.; Morawiec, A.; **Ubar, Raimund-Johannes** Techniques of Informatics and Microelectronics for Computer Architecture 1999 / p. 91-94

Microprocessor modeling for board level test access automation
Devadze, Sergei; **Jutman, Artur**; Tšertov, Anton; **Ubar, Raimund-Johannes** Proceedings of 10th IEEE Workshop on RTL and High Level Testing : Hong Kong, November 27-28, 2009 2009 / ? p

Microprocessor-based system test using debug interface
Devadze, Sergei; **Jutman, Artur**; **Tšertov, Anton**; Instenberg, Martin; **Ubar, Raimund-Johannes** 26th Norchip Conference : Tallinn, Estonia, 17-18 November 2008 : formal proceedings 2008 / p. 98-101 : ill http://dx.doi.org/10.1109/NORCHP.2008.4738291

Mida peaks teaduspoliitikas reformima? : kui hindamisel jääb puudu kompetentsusest, on bibliomeetria see faktor, mis alati kõneleb täiel häälel ja vastuvaidlematult
Ubar, Raimund-Johannes Sirp 2014 / lk. 34-35 https://www.sirp.ee/s1-artiklid/c9-sotsiaalia/mida-peaks-teaduspoliitikas-reformima/

Mikroprotsessor Tehnikaülikoolist transistori 50. sünnipäevaks
Ubar, Raimund-Johannes Horisont 1997 / 8, lk. 10-11: ill https://artiklid.elnet.ee/record=b2325971*est

Miks on oskus kiipe luua Eesti jaoks oluline?
Raik, Jaan; **Ubar, Raimund-Johannes** postimees.ee 2025 https://arvamus.postimees.ee/8313767/jaan-raik-raimund-ubar-miks-on-oskus-kiipe-luua-eesti-jaoks-oluline

Minicomputer software for fault location control in digital circuits
Lohuaru, Tõnu; **Viilup, Agu**; **Ubar, Raimund-Johannes** Preprints the 2nd IFAC/IFIP Symposium on Software for Computer Control, SOCOCO, Prague, Czechoslovakia, June 11-15, 1979 ; Vol. 1 1979 / p. [?] https://www.ester.ee/record=b2041567*est

Minimization of the high-level fault model for microprocessor control parts [Online resource]

Ubar, Raimund-Johannes; **Oyeniran, Adeboye Stephen**; **Medaiyese, Olusiji** BEC 2018 : 2018 16th Biennial Baltic Electronics Conference (BEC) : proceedings of the 16th Biennial Baltic Electronics Conference, October 8-10, 2018 2018 / 4 p.: ill
https://doi.org/10.1109/BEC.2018.8600980

Missioonikriitiliste sardsüsteemide arendamise nimel : [Integreeritud Elektroonikasüsteemide ja Biomeditsiinitehnika Tippkeskusest : intervjuu Raimund Ubari ja Gert Jervaniga]
Ubar, Raimund-Johannes; **Jervan, Gert**; **Ummelas, Mart** Mente et Manu 2009 / 30. jaan., lk. 1, 3 : ill ; 16. veebr., lk. 5 : ill
https://www.ester.ee/record=b1242496*est

Mixed bottom-up/top-down hierarchical test generation for digital systems
Ubar, Raimund-Johannes Proceedings of the 9th European Workshop on Dependable Computing, Gdansk, Poland, May 14-16, 1998 1998 / p. 37-40

Mixed hierarchical-functional fault models for targeting sequential cores
Raik, Jaan; **Ubar, Raimund-Johannes**; **Viilukas, Taavi**; **Jenihhin, Maksim** Journal of systems architecture 2008 / 3/4, p. 465-477 : ill https://www.sciencedirect.com/science/article/abs/pii/S1383762107001166

Mixed-level defect simulation in data-paths of digital systems
Ubar, Raimund-Johannes; **Raik, Jaan**; **Ivask, Eero**; **Brik, Marina** 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 617-620 : ill https://ieeexplore.ieee.org/document/1003333

Mixed-level deterministic-random test generation for digital systems
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 335-340

Mixed-level identification of fault redundancy in microprocessors
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Gürsoy, Cemil Cem**; **Raik, Jaan** LATS 2019 : 20th IEEE Latin American Test Symposium : Santiago, Chile, March 11th - 13th 2019 2019 / 6 p. : ill
https://doi.org/10.1109/LATW.2019.8704591

Mixed-level test generator for digital systems
Brik, Marina; **Jervan, Gert**; **Markus, Antti**; **Paomets, Priidu**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the Estonian Academy of Sciences. Engineering 1997 / 4, p. 271-282 : ill

Modeling and simulation of circuits with shared structurally synthesized BDDs
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Raik, Jaan**; **Viies, Vladimir** Microprocessors and microsystems 2017 / p. 56-61 : ill
https://doi.org/10.1016/j.micpro.2016.09.006 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Modeling microprocessor faults on high-level decision diagrams [Electronic resource]
Ubar, Raimund-Johannes; **Raik, Jaan**; **Jutman, Artur**; **Jenihhin, Maksim**; Istenberg, Martin; Wuttke, Heinz-Dietrich DSN 2008 : supplemental : 2008 IEEE International Conference on Dependable Systems & Networks With FTCS & DCC (DSN) : June 24-27, 2008, Anchorage, Alaska 2008 / p. C17-C22 : ill. [CD-ROM]
https://webhost.laas.fr/TSF/WDSN08/2ndWDSN08(LAAS)_files/Slides/WDSN08S-04-Ubar.pdf

Modeling sequential circuits with shared structurally synthesized BDDs
Ubar, Raimund-Johannes; **Marenkov, Mihhail**; **Mironov, Dmitri**; **Viies, Vladimir** Proceedings of 2014 9th International Design & Test Symposium (IDT) : Sheraton Club des Pins Hotel, Algiers, Algeria, December 16-18, 2014 2014 / p. 130-135 : ill

Module level defect simulation in digital circuits
Kuzmicz, Wieslaw; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the Estonian Academy of Sciences. Engineering 2001 / 4, p. 253-268

Module-level fault diagnosis in combinational networks
Ubar, Raimund-Johannes Fault-tolerant systems and diagnostics : FTSD 1978 / p. 297-314

Momentvõtteid Eesti Teadusfondi 10-aastaselt teelt : [koosolekute protokollide ja ülestähenduste põhjal]
Veiderma, Mihkel; **Aarna, Olav**; **Ubar, Raimund-Johannes**; **Tamm, Boris, inform.** 2001 https://www.ester.ee/record=b1476103*est

Multi-level fault simulation of digital systems on decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Ivask, Eero**; **Brik, Marina** The First IEEE International Workshop on Electronic Design, Test and Applications : DELTA 2002, 29-31 January 2002, Christchurch, New Zealand : proceedings 2002 / p. 86-91 : ill

Multi-level test generation and fault diagnosis for finite state machines
Ubar, Raimund-Johannes; **Brik, Marina** Dependable computing : proceedings / EDCC-2, Second European Dependable Computing Conference, Taormina, Italy, October 2-4, 1996 1996 / p. 264-281: ill

Multi-level test generation and fault diagnosis in digital systems
Ubar, Raimund-Johannes 1992

Multi-level test generation for digital systems at system, circuit and defect levels
Ubar, Raimund-Johannes Proceedings of the 7th International Scientific Conference "Theory and Technique of Information Transmission, Reception and Processing" : Tuapse, October 1-4, 2001 2001 / p. 286-288

Multiple control fault testing in digital systems with high-level decision diagrams
Ubar, Raimund-Johannes; **Oyeniran, Adeboye Stephen** 2016 IEEE International Conference on Automation, Quality and Testing, Robotics (AQTR) : THETA 20th edition : 19th-21st May, Cluj-Napoca, Romania : proceedings 2016 / [6] p. : ill
http://dx.doi.org/10.1109/AQTR.2016.7501287

Multiple fault analyses in logic circuits
Ubar, Raimund-Johannes IFAC-Symposium Discrete Systems : Dresden, 14.-19. 3. 77 1977 / p. [?]

Multiple fault diagnosis with BDD based Boolean differential equations
Ubar, Raimund-Johannes; **Raik, Jaan**; **Kostin, Sergei**; Kõusaar, Jaak BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 77-80 : ill

Multiple fault testing in systems-on-chip with high-level decision diagrams
Ubar, Raimund-Johannes; **Oyeniran, Adeboye Stephen**; Schölzel, Mario; Vierhaus, Heinrich Theodor Proceedings of 2015 10th International Design & Test Symposium (IDT) : Dead Sea, Jordan, 14-16 December 2015 2015 / p. 66-71 : ill
http://dx.doi.org/10.1109/IDT.2015.7396738

Multiple stuck-at-fault detection theorem
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 236-241 : ill

Multi-valued simulation of digital circuits
Ubar, Raimund-Johannes Proceedings : 1997 21st International Conference on Microelectronics : Niš, Yugoslavia, 14-17 September 1997. Vol. 2 1997 / p. 721-724 : ill

Multi-valued simulation of digital circuits with structurally synthesized binary decision diagrams
Ubar, Raimund-Johannes Multiple valued logic. Vol. 4 1998 / p. 141-157

Multivalued simulation on AG-model of digital devices
Ubar, Raimund-Johannes; Voolaine, Andrus Proceedings of the 12th Conference on Fault-Tolerant Systems and Diagnostics, Prague, Czechoslovakia, September, 1989 1989 / p. 101-104

Multi-valued simulation with binary decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan** Proceedings IEEE European Test Workshop, Cagliari, Italy, May 28-30, 1997 1997 / p. 28-29

Mutation analysis for systemC designs at TLM
Guarnieri, Valerio; Bombieri, Nicola; Pravadelli, Graziano; Fummi, Franco; **Hantson, Hanno**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes** 12th IEEE Latin American Test Workshop (LATW) : Porto de Galinhas, Brasil, 27-30 March 2011 2011 / [6] p
https://ieeexplore.ieee.org/document/5985925

Mutation analysis with high-level decision diagrams
Hantson, Hanno; **Raik, Jaan**; **Jenihhin, Maksim**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes**; Guglielmo, Giuseppe di; Fummi, Franco LATW2010 : 11th Latin-American TestWorkshop, March 28-31, 2010, Punta del Este, Uruguay 2010 / [6] p. [CD-ROM] https://ieeexplore.ieee.org/document/5550336

Mõtted TTÜ arengukava koostamise puhul
Ubar, Raimund-Johannes Tehnikaülikool 1999 / 17. mai, lk. 5-8 https://www.ester.ee/record=b5309277*est

Mõtteid koostöö võimalikkusest Ida-Lääne piiril
Ubar, Raimund-Johannes; **Kruus, Margus** Mente et Manu 2003 / 20. okt., lk. 2 : portr https://artiklid.elnet.ee/record=b1415646*est

Mõtteid kõrgharidus- ja teaduspoliitilisest olukorrast Eestis
Ubar, Raimund-Johannes Eesti Teaduste Akadeemia aastaraamat 2000 2001 / lk. 135-139

Nanoelectronics aging mitigation using SSBDD based techniques and dedicated sensors
Ubar, Raimund-Johannes; Vargas, Fabian; **Jenihhin, Maksim**; **Raik, Jaan** MEDIAN Workshop on Circuit Reliability : Modeling and Monitoring, Rome, Italy, February 25, 2013 2013 / [1] p

New built-in self-test scheme for SoC interconnect
Jutman, Artur; **Ubar, Raimund-Johannes**; **Raik, Jaan** The 9th World Multi-Conference on Systemics, Cybernetics and Informatics : WMSCI 2005 : July 10-13, 2005, Orlando, Florida, USA. Vol. IV 2005 / p. 19-24 : ill
https://www.researchgate.net/publication/237375234_New_Built-In_Self-Test_Scheme_for_SoC_Interconnect

New categories of Safe Faults in a processor-based Embedded System
Gürsoy, Cemil Cem; **Jenihhin, Maksim**; **Oyeniran, Adeboye Stephen**; Piumatti, Davide; **Raik, Jaan**; Sonza Reorda, Matteo; **Ubar, Raimund-Johannes** 2019 22nd International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS), Cluj-Napoca, Romania : proceedings 2019 / 4 p. : ill https://doi.org/10.1109/DDECS.2019.8724642

New curricula and a competence centre through TEMPUS at the Technical University of Tallinn
Glesner, M.; Hollstein, Thomas; Courtois, B.; Amblar, P.; **Ubar, Raimund-Johannes**; **Vainomaa, Kaido** Workshop on Design Methodologies for Microelectronics, Smolenice castle, Slovakia, September 11-13, 1995 : proceedings 1995 / p. 347-353

New fault models and self-test generation for microprocessors using High-Level Decision Diagrams
Jasnetski, Artjom; **Raik, Jaan**; **Tšertov, Anton**; **Ubar, Raimund-Johannes** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 251-254 : ill

A new measure for calculating multiple fault coverage of microprocessor self-test
Oyeniran, Adeboye Stephen; **Odozi, Uzochukwu Eddie**; **Ubar, Raimund-Johannes** BEC 2016 : 2016 15th Biennial Baltic Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-5, 2016, Tallinn, Estonia 2016 / p. 75-78 : ill http://www.ester.ee/record=b2150914*est

New method of testability calculation to guide RT-level test generation
Raik, Jaan; **Nõmmeots, Tanel**; **Ubar, Raimund-Johannes** 4th IEEE Latin-American Test Workshop : LATW2003 : Natal, Brazil, February 16-19, 2003 2003 / p. 46-51 : ill https://link.springer.com/article/10.1007/s10836-005-5288-5

New technique for hierarchical identification of untestable faults in sequential circuits
Krivenko, Anna; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Kruus, Margus** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / lk. 155-158 : ill

New test design techniques for fault detection in digital objects
Alango, Villem; **Kont, Toomas**; **Ubar, Raimund-Johannes** Tallinna Tehnikaülikooli Toimetised 1990 / lk. 45-62: ill

A novel artificial neural networks based automatic adaptive fault detection technique for analog circuits
Petlenkov, Eduard; **Jutman, Artur**; **Nõmm, Sven**; **Ubar, Raimund-Johannes** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 167-170 : ill

A novel random approach to diagnostic test generation
Osimiry, Emmanuel Ovie; **Ubar, Raimund-Johannes**; **Kostin, Sergei**; **Raik, Jaan** 2nd IEEE NORCAS Conference : 1-2 November 2016, Copenhagen, Denmark 2016 / [4] p. : ill https://doi.org/10.1109/NORCHIP.2016.7792915

Off-line testing of crosstalk induced glitch faults in NoC Interconnects
Bengtsson, Tomas; Kumar, Shashi; **Jutman, Artur**; **Ubar, Raimund-Johannes** Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 221-225 : ill http://dx.doi.org/10.1109/NORCHP.2006.329215

Off-line testing of delay faults in NoC interconnects
Bengtsson, Tomas; **Jutman, Artur**; Kumar, Shashi; Peng, Zebo; **Ubar, Raimund-Johannes** 9th EUROMICRO Conference on Digital Systems Design : Architectures, Methods and Tools (DSD 2006) : 30 August 2006-1 September 2006, Cavtat near Dubrovnik, Croatia : proceedings 2006 / p. 677-680 : ill http://dx.doi.org/10.1109/DSD.2006.72

On automatic software-based self-test program generation based on high-Level decision diagrams
Jasnetski, Artjom; **Ubar, Raimund-Johannes**; **Tšertov, Anton** LATS 2016 : 17th IEEE Latin-American Test Symposium, Foz do Iguacu, Brazil, 6th-9th April 2016 2016 / p. 177 http://dx.doi.org/10.1109/LATW.2016.7483357

On efficient logic-level simulation of digital circuits represented by the SSBDD model
Jutman, Artur; **Raik, Jaan**; **Ubar, Raimund-Johannes** 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings. Volume 2 2002 / p. 621-624 : ill https://ieeexplore.ieee.org/document/1003334

On reusability of verification assertions for testing
Jenihhin, Maksim; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Tšepurov, Anton** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 151-154 : ill

On test generation for microprocessors for extended class of functional faults
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim**; **Raik, Jaan** VLSI-SoC: New technology enabler : 27th IFIP WG 10.5/IEEE International Conference on Very Large Scale Integration, VLSI-SoC 2019 Cusco, Peru, October 6–9, 2019 : Revised and Extended Selected Papers 2020 / p. 21-44 https://doi.org/10.1007/978-3-030-53273-4 Conference proceedings at Scopus Article at Scopus

On the combined use of HLDDs and EFSMs for functional ATPG
Di Guglielmo, Giuseppe; Fummi, Franco; **Jenihhin, Maksim**; Pravadelli, Graziano; **Raik, Jaan**; **Ubar, Raimund-Johannes** 5th IEEE East-West Design & Test Symposium EWDTS 2007 : September 7-10, 2007, Yerevan, Armenia 2007 / p. 503-508 : ill

On the reuse of TLM mutation analysis at RTL
Guarnieri, Valerio; **Hantson, Hanno**; **Raik, Jaan**; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2012 / p. 435-448 : ill https://link.springer.com/article/10.1007/s10836-012-5303-6

On using genetic algorithm for test generation
Brik, Marina; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Ivask, Eero** BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 233-236 : ill

On-line monitoring of dialysis adequacy using diasens optical sensor: accurate Kt/V estimation by smoothing algorithms
Talisainen, Aleksei; **Kostin, Sergei**; **Karai, Deniss**; **Fridolin, Ivo**; **Ubar, Raimund-Johannes** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 273-276 : ill

Open-source JTAG simulator bundle for labs
Shibin, Konstantin; **Devadze, Sergei**; **Rosin, Vjatšeslav**; **Jutman, Artur**; **Ubar, Raimund-Johannes** International journal of electronics and telecommunications 2012 / p. 233-239 : ill https://journals.pan.pl/Content/87192/PDF/32.pdf

Operatsioonautomaadid digitaalarvutites : metoodiline materjal
1987 https://www.ester.ee/record=b1234461*est

Optimierte Steuerung der Fehlersuche auf digitalen Leiterplatten
Thomä, E.; **Ubar, Raimund-Johannes** Proceedings of the 27th International Conference, Technical University of Ilmenau, October, 1982 1982 / p. 65-68

Optimization of built-in self-test in digital systems = Sisseehitatud enesetestimise optimeerimine digitaalsüsteemides
Kruus, Helena 2011

Optimization of memory-constrained hybrid BIST for testing core-based systems
Jervan, Gert; **Kruus, Helena**; **Orasson, Elmet**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 133-136 : ill

Optimization of memory-constrained hybrid BIST for testing core-based systems
Jervan, Gert; **Kruus, Helena**; **Orasson, Elmet**; **Ubar, Raimund-Johannes** Proceedings of the IEEE 2nd International Symposium on Industrial Embedded Systems : SIES'2007 : Lisbon, Portugal, 4-6 July 2007 2007 / p. 71-77
https://ieeexplore.ieee.org/document/4297319

Optimization of structurally synthesized BDDs
Ubar, Raimund-Johannes; Vassiljeva, T.; **Raik, Jaan**; **Jutman, Artur**; Tombak, Mati; Peder, Ahti Proceedings of the Fourth IASTED International Conference on Modelling, Simulation, and Optimization : August 17-19, 2004, Kavai, Hawaii, USA 2004 / p. 234-240 : ill https://www.academia.edu/22101496/Optimization_of_structurally_synthesized_BDDs

Optimization of the store-and-generate based built-in self-test
Ubar, Raimund-Johannes; **Jervan, Gert**; **Kruus, Helena**; **Orasson, Elmet**; **Aleksejev, Igor** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 199-202 : ill

Otstarbeka, õiglase ja efektiivse Eesti eest
Ubar, Raimund-Johannes Tehnikaülikool 1995 / 23. jaan., lk. 3-5 https://www.ester.ee/record=b5309277*est

Otstarbeka, õiglase ja tõhusa Eesti suunas
Ubar, Raimund-Johannes Inseneerikultuur Eestis. 2 1995 / lk. 179-185 https://www.ester.ee/record=b1063622*est

Overview about low-level and high-level decision diagrams for diagnostic modeling of digital systems
Ubar, Raimund-Johannes Facta Universitatis [Niš]. Series electronics and energetics 2011 / p. 303-324 : ill
http://dx.doi.org/10.2298/FUEE1103303U

Overview about low-lewel and high-level decision diagrams for diagnostic modeling of digital systems
Ubar, Raimund-Johannes Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 1-10 : ill
https://scindeks-clanci.ceon.rs/data/pdf/0353-3670/2011/0353-36701103303U.pdf

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems
Jutman, Artur; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Microelectronics education : proceedings of the 5th European Workshop on Microelectronics Education, held in Lausanne, Switzerland, April 15-16, 2004 2004 / p. 253-258 : ill
https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Overview of e-learning environment for web-based study of testing and diagnostics of digital systems
Jutman, Artur; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 5th European Workshop on Microelectronics Education - EWME 2004, Lausanne, 2004 2004 / p. 173-176 https://link.springer.com/chapter/10.1007/978-1-4020-2651-5_41

Parallel critical path tracing fault simulation
Ubar, Raimund-Johannes 39. Internationales Wissenschaftliches Kolloquium : 27.-30.09.1994. Bd. 1, Vortragsreihen 1994 / S. 399-404

Parallel critical path tracing fault simulation in sequential circuits
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Kostin, Sergei**; **Devadze, Sergei**; **Raik, Jaan** Proceedings of 25th International Conference MIXED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS : MIXDES 2018 : Gdynia, Poland, June 21–23, 2018 2018 / p. 305-310 : ill https://doi.org/10.23919/MIXDES.2018.8436880

Parallel exact critical path tracing fault simulation with reduced memory requirements
Devadze, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Jutman, Artur** 4th International Conference on Design and Technology of Integrated Systems in Nanoscal Era : DTIS'09 : Cairo, Egypt, April 6-9, 2009 2009 / p. 155-160 : ill
https://ieeexplore.ieee.org/document/4938046

Parallel fault analysis on structurally synthesized BDDs
Devadze, Sergei; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 47-50 : ill

Parallel fault backtracing for calculation of fault coverage
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 43rd International Conference on Microelectronics, Devices and Materials and the Workshop on Electronic Testing : September 12. - September 14.2007, Bled, Slovenia : MIDEM conference 2007 proceedings 2007 / p. 165-170 : ill
https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault backtracing for calculation of fault coverage
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** Proceedings of the ASP-DAC 2008 : [13th] Asia and South Pacific Design Automation Conference 2008 : January 21-24, 2008, COEX, Seoul, Korea 2008 / p. 667-672 : ill
https://www.researchgate.net/publication/221153650_Parallel_fault_backtracing_for_calculation_of_fault_coverage

Parallel fault simulation in digital circuits
Aarna, Margit; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proc. of 42nd International Scientific Conference of Riga Technical University 2001 / p. 91-94

Parallel fault simulation in digital circuits
Aarna, Margit; **Raik, Jaan**; **Ubar, Raimund-Johannes** Scientific proceedings of Riga Technical University. 7. serija, Telecommunications and electronics 2001 / p. 91-94 : ill

Parallel pseudo-exhaustive testing of array multipliers with data-controlled segmentation
Oyeniran, Adeboye Stephen; **Azad, Siavoosh Payandeh**; **Ubar, Raimund-Johannes** 2018 IEEE International Symposium on Circuits and Systems (ISCAS) : 27-30 May 2018, Florence, Italy : proceedings 2018 / 5 p.: ill
https://doi.org/10.1109/ISCAS.2018.8350936 Conference proceedings at Scopus Article at Scopus Article at WOS

Parallel X-fault simulation with critical path tracing technique [Electronic resource]
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** DATE 10 : Design, Automation & Test in Europe : Dresden, Germany, 8-12 March, 2010 2010 / p. 879-884 [CD-ROM] https://www.researchgate.net/publication/221341788_Parallel_X-fault_simulation_with_critical_path_tracing_technique

Pildikesi poolest sajandist : arvutitehnika instituudi lugu
Ubar, Raimund-Johannes 2016 http://www.ester.ee/record=b4639382*est

Pipelined execution of data-parallel algorithms
Gorev, Maksim; **Ubar, Raimund-Johannes** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 109-112 : ill

Practical works for on-line teaching design and test of digital circuits
Jutman, Artur; **Ubar, Raimund-Johannes**; Hahanov, V.; Skvortsova, O. The 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS 2002 : September 15-18, 2002, Dubrovnik, Croatia. Volume III 2002 / p. 1223-1226 : ill
http://dx.doi.org/10.1109/ICECS.2002.1046474

Preface
Ubar, Raimund-Johannes; **Raik, Jaan**; Vierhaus, Heinrich Theodor Design and test technology for dependable systems-on-chip 2011 / p. xxii-xxviii

Preface
Lyapin, Alexandr; Murgul, Vera; Beskopylny, A.N.; Porksheyan, V.M.; Komakhidze, M.G.; Sukhinov, A.I.; Chetverushkin, B.N.; Avetisyan, A.I.; Kalyaev, I.A; **Ubar, Raimund-Johannes** Journal of Physics: Conference Series 2021 / art. 011001, 1 p
https://doi.org/10.1088/1742-6596/2131/1/011001 Conference proceedings at Scopus Article at Scopus

Probabilistic analysis of CMOS physical defects in VLSI circuits for test coverage improvement
Blyzniuk, M.; Kazymyra, I.; Kuzmicz, W.; Pleskacz, Witold A.; **Raik, Jaan**; **Ubar, Raimund-Johannes** Microelectronics reliability 2001 / p. 2023-2040 : ill https://www.sciencedirect.com/science/article/pii/S0026271401000920

Probabilistic equivalence checking based on high-level decision diagrams
Karputkin, Anton; **Ubar, Raimund-Johannes**; **Tombak, Mati**; **Raik, Jaan** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 423-428 : ill
https://ieeexplore.ieee.org/document/5783130

Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia
2012 http://www.ester.ee/record=b2777270*est

Professor Raimund Ubari ettekanne [audoktorite promotsioonil TTÜ Nõukogu pidulikul istungil 1. sept. 1993]
Ubar, Raimund-Johannes 75 aastat Tallinna Tehnikaülikooli 1994 / lk. 106-109 https://www.ester.ee/record=b1066846*est

A proposal for optimisation of low-powered FSM testing
Brik, Marina; **Fomina, Jelena**; **Ubar, Raimund-Johannes** Proceedings of IEEE East-West Design & Test Workshop (EWDTW'05) : Odessa, Ukraine, September 15-19, 2005 2005 / p. 15-20

PSL assertion checking using temporally extended high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Journal of electronic testing : theory and applications 2009 / 6, p. 289-300 : ill https://pld.ttu.ee/home/maksim/phd_papers/%5B11%5D%20latw%2708.pdf

PSL assertion checking with temporally extended high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings of the 9th IEEE Latin-American Test Workshop : LATW2008 : February 17-20, 2008, Puebla, Mexico 2008 / p. 49-54 : ill
https://pld.ttu.ee/~maksim/phd_papers/%5B11%5D%20latw%2708.pdf

Pöidlasuurune hiiglane
Ubar, Raimund-Johannes Sõnumileht 1998 / 1. märts, lk. 8: ill https://artiklid.elnet.ee/record=b1761233*est

Pöördumine Haridus- ja Teadusministri ning Riigikogu kultuurikomisjoni esimehe poole : [doktorikoolide probleemist]
Arro, Ilmar; **Kaljurand, Mihkel**; **Kallavus, Urve**; **Kübarsepp, Jakob**; **Lille, Ülo**; **Lopp, Margus**; **Mellikov, Enn**; **Min, Mart**; **Rang, Toomas**; **Rüstern, Ennu**; **Taklaja, Andres**; **Tamm, Toomas**; **Tammet, Tanel**; **Tepandi, Jaak**; **Ubar, Raimund-Johannes**; **Öpik, Andres** Mente et Manu 2005 / 18. mai. lk. 1 https://www.ester.ee/record=b1242496*est

Pöördumine Haridus- ja Teadusministri ning Riigikogu kultuurikomisjoni esimehe poole : [doktorikoolide probleemist]
Arro, Ilmar; **Kaljurand, Mihkel**; **Kallavus, Urve**; **Kübarsepp, Jakob**; **Lille, Ülo**; **Lopp, Margus**; **Mellikov, Enn**; **Min, Mart**; **Rang, Toomas**; **Rüstern, Ennu**; **Taklaja, Andres**; **Tamm, Toomas**; **Tammet, Tanel**; **Tepandi, Jaak**; **Ubar, Raimund-Johannes**; **Öpik, Andres** Tallinna Tehnikaülikooli aastaraamat 2005 2006 / lk. 430-431

Quo vadis, tehnikakõrgharidus? : [kõne inseneride päeva tähistamisel Eesti Inseneride Liidus 9. detsembril 2011 Eesti Teaduste Akadeemia saalis Toompeal]
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2011 2012 / lk. 296-307

Rahvusvaheline konverents ja magistrikraadid
Ubar, Raimund-Johannes Tehnikaülikool 1997 / 1. dets., lk. 3: ill https://www.ester.ee/record=b5309277*est

Raimund Ubari lühisõnavõtt : riigi teadus-, kultuuri- ja spordipreemiate ning F.J.Wiedemanni keeleauhinna kätteandmisel 24. veebruaril 2016. aastal

Ubar, Raimund-Johannes Raimund-Johannes Ubar. Bibliograafia 2016 / lk. 45-46

Register-transfer level deductive fault simulation using decision diagrams
Reinsalu, Uljana; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 193-196 : ill

Reisikirjad võõrsilt
Ubar, Raimund-Johannes Horisont 1995 / 1, lk. 54-58; 2, lk. 35-39; 3, lk. 59-62; 4, lk. 51-54; 5, lk. 51-54; 6, lk. 51-55: ill https://artiklid.elnet.ee/record=b2029755*est

Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs
Pellerey, Francesco; **Jenihhin, Maksim**; Squillero, Giovanni; **Raik, Jaan**; Sonza Reorda, Matteo; **Tihhomirov, Valentin**; **Ubar, Raimund-Johannes** 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill https://doi.org/10.1109/ATS.2016.57 Conference Proceedings at Scopus Article at Scopus Article at WOS

Rektor Andres Keevallik saab 24. veebruaril 70aastaseks
Hazak, Gabriel; **Ubar, Raimund-Johannes**; **Kattel, Rainer** Mente et Manu 2013 / lk. 16 : fot https://www.ester.ee/record=b1242496*est

Remarks on different decision diagrams
Stankovic, Radomir S.; **Ubar, Raimund-Johannes**; Astola, Jaakko Proceedings of the Reed-Muller 2011 Workshop : May 25-26, 2011, Tuusula, Finland 2011 / p. 99-110 : ill

Remote and virtual laboratories in problem-based learning scenarios
Wuttke, Heinz-Dietrich; **Ubar, Raimund-Johannes**; Henke, Karsten 2010 IEEE International Symposium on Multimedia ISM 2010 : 13-15 December 2010, Taichung, Taiwan : proceedings 2010 / p. 377-382 : ill http://dx.doi.org/10.1109/ISM.2010.63

Removing design errors from digital circuits
Ubar, Raimund-Johannes Proc. of the 4th International Conference on New Information Technologies. Vol. 1 2000 / p. 118-125

Replication-based deterministic testing of 2-dimensional arrays with highly interrelated cells
Azad, Siavoosh Payandeh; **Oyeniran, Adeboye Stephen**; **Ubar, Raimund-Johannes** 21st IEEE International Symposium on Design and Diagnostics of Electronic Circuits and Systems : DDECS 2018 : Budapest, Hungary 25-27 April, 2018 : proceedings 2018 / p. 21-26 : ill https://doi.org/10.1109/DDECS.2018.00011

Representing gate-level SET faults by multiple SEU faults on RT-level
Bagbaba, Ahmet Cagri; **Jenihhin, Maksim**; **Ubar, Raimund-Johannes**; Sauer, Christian 2020 IEEE 26th International Symposium on On-Line Testing and Robust System Design (IOLTS), 13-15 July 2020 : proceedings 2020 / art. 19889351, 6 p. : ill https://doi.org/10.1109/IOLTS50870.2020.9159715

Representing transparency conditions in test generation for VLSI by decision diagrams
Ubar, Raimund-Johannes Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 213-216

Research and training environment for digital design and test
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 34th ASEE/IEEE Frontiers in Education Conference : October 20-23, 2004, Savannah, GA 2004 / p. S3F-18-S3F-23 : ill http://dx.doi.org/10.1109/FIE.2004.1408779

Research and training environment for digital design and test
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the Eighth IASTED International Conference on Computers and Advanced Technology in Education : August 29-31, 2005, Oranjestad, Aruba 2005 / p. 232-237 : ill https://ieeexplore.ieee.org/document/1408779

Research and training scenarios for design and test of SOC [Electronic resource]
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich WCETE 2004 : World Congress on Engineering and Technology Education : Engineering Education in the Changing Society : March 14-17, 2004, Guaruja/Santos, Brazil 2004 / p. 320-324 : ill. [CD-ROM]

Research environment for teaching digital test
Ivask, Eero; **Jutman, Artur**; **Orasson, Elmet**; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Synergies between Information and Automation : 49. Internationales Wissenschaftliches Kolloquium, 27.-30.9.2004, Technische Universität Ilmenau, Germany. Volume 2 2004 / p. 468-473 : ill https://pld.ttu.ee/dildis/publications/IWK'2004_res_inv.pdf

Research in digital design and test at Tallinn University of Technology
Ubar, Raimund-Johannes; **Jervan, Gert**; **Jutman, Artur**; **Raik, Jaan**; **Ellervee, Peeter**; **Kruus, Margus** Radioelectronics & informatics 2008 / p. 4-12 : ill http://www.ewdtest.com/ri/%E2%84%96-1-40-january-march-2008/

Research on digital system design and test at Tallinn University of Technology
Ubar, Raimund-Johannes; **Ellervee, Peeter**; **Hollstein, Thomas**; **Jervan, Gert**; **Jutman, Artur**; **Kruus, Margus**; **Raik, Jaan**
Research in Estonia : present and future 2011 / p. 184-205 : ill

Reseeding using compaction of pre-generated LFSR sequences
Jutman, Artur; **Aleksejev, Igor**; **Raik, Jaan**; **Ubar, Raimund-Johannes** ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : 31st August to 3rd September 2008, Malta : conference guide 2008 / p. 215

Reseeding using compaction of pre-generated LFSR sub-sequences
Jutman, Artur; **Aleksejev, Igor**; **Raik, Jaan**; **Ubar, Raimund-Johannes** ICECS 2008 : The 15th IEEE International Conference on Electronics, Circuits and Systems : Malta 2008 / p. 1290-1295 : ill http://dx.doi.org/10.1109/ICECS.2008.4675096

Results of international cooperation for development and exchange of web-based educational materials
Gramatova, Elena; **Ubar, Raimund-Johannes** Proceedings of the III International Conference "Distance Learning - Educational Sphere of XXI Century" : Minsk, Belorussia, 2003 2003 / p. 17-23

RT-level test point insertion for sequential circuits
Raik, Jaan; Govind, Vineeth; **Ubar, Raimund-Johannes** IWoTA 2004 : IEEE 1st International Workshop on Testability Assessment : November 2, 2004, Rennes, France : proceedings 2004 / p. 34-40 : ill https://ieeexplore.ieee.org/document/1428412

Salajane teadus Eestis
Ubar, Raimund-Johannes Tallinna Ülikoolid 1998 / 2, lk. 38-39

Scalable algorithm for structural fault collapsing in digital circuits
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Orasson, Elmet**; **Raik, Jaan** 2015 IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC) : October 5-7, 2015, Daejeon, Korea 2015 / p. 171-176 : ill

A scalable technique to identify true critical paths in sequential circuits
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Jenihhin, Maksim**; **Raik, Jaan** Proceedings 2017 IEEE 20th International Symposium on Design and Diagnotics of Electronic Circuit & Systems(DDECS) : April 19-21, 2017, Dresden, Germany 2017 / p. 152-157 : ill
https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7934553

Second IEEE East-West Design and Test Workshop
Hahanov, Vladimir; **Ubar, Raimund-Johannes** IEEE journal of design & test of computers 2004 / p. 594

Selected issues of modeling, verification and testing of digital systems
Jutman, Artur 2004 https://www.ester.ee/record=b1989760*est

Selected papers from the 1997 NORCHIP conference
Lande, Tor Sverre; **Ubar, Raimund-Johannes** 1999

Self-diagnosis in digital systems = Isediagnoosivad digitaalsüsteemid
Kostin, Sergei 2012 https://www.ester.ee/record=b2757857*est

Self-learning tool for digital test
Ubar, Raimund-Johannes; **Orasson, Elmet**; **Evartson, Teet** Proceedings of 2nd International Conference "Distance Learning - Educational Sphere of the XXI Century" 2002 / p. 36-38 : ill

Self-testing of pipe-lined signal processing architectures at-speed
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 25-28 : ill

Sequential circuit test generation using decision diagram models
Raik, Jaan; **Ubar, Raimund-Johannes** Design, Automation and Test in Europe : DATE : Conference and Exhibition 1999 : Munich, Germany, March 9-12, 1999 : proceedings 1999 / p. 736-740: ill https://www.cs.york.ac.uk/rts/docs/SIGDA-Compendium-1994-2004/papers/1999/date99/pdffiles/11e_1.pdf

Sequential circuits BIST with status bit control
Raik, Jaan; **Orasson, Elmet**; **Ubar, Raimund-Johannes** Proceedings of the 11th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2004 : Szczecin, Poland, 24-26 June 2004 2004 / p. 507-510 : ill
https://pld.ttu.ee/~raiub/files/aaaaa_pulk/MIXDES/jaan.pdf

A set of tools for estimating quality of built-in self-test in digital circuits
Jervan, Gert; **Markus, Antti**; **Paomets, Priidu**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the International Symposium on Signals, Circuits and Systems, Iasi (Romania), October 2-3, 1997 1997 / p. 362-365

7-valued algebra for transition delay fault analysis
Kõusaar, Jaak; **Ubar, Raimund-Johannes** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 89-92 : ill

Shared Structurally Synthesized BDDs for speeding-up parallel pattern simulation in digital circuits
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Raik, Jaan** 2015 Nordic Circuits and Systems Conference (NORCAS) : NORCHIP & International Symposium on System-on-Chip (SoC) : 1st IEEE NORCAS Conference : 26-28 October 2015, Oslo, Norway 2015 / [4] p. : ill http://dx.doi.org/10.1109/NORCHIP.2015.7364406

Simulating system for minicomputer diagnostic programs
Kitsnik, Peeter; **Ubar, Raimund-Johannes**; **Viilup, Agu** Preprints 1st IFAC/IFIP Symposium on Software for Computer Control, SOCOCO-76 : Tallinn, USSR, May 25-28, 1976 1976 / lk. [?] https://www.ester.ee/record=b1291026*est http://www.digar.ee/id/nlib-digar:451346

Simulation of digital systems with high-level decision diagrams
Morawiec, Adam; **Raik, Jaan**; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 35-38 : ill

Simulation-based hardware verification with high-level decision diagrams = Simuleerimisel põhinev riistvara verifitseerimine kõrgtaseme otsustusdiagrammidel
Jenihhin, Maksim 2008 https://www.ester.ee/record=b2431332*est

Simulation-based verification with APRICOT framework using high-level decision diagrams
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 13-16 : ill

Single gate design error diagnosis in combinational circuits
Ubar, Raimund-Johannes; Borrione, Dominique Proceedings of the Estonian Academy of Sciences. Engineering 1999 / 1, p. 3-21: ill https://artiklid.elnet.ee/record=b1000315*est

SoC and board modeling for processor-centric board testing
Tšertov, Anton; **Ubar, Raimund-Johannes**; **Jutman, Artur**; **Devadze, Sergei** 14th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2011 : 31 August - 2 September 2011, Oulu, Finland : proceedings 2011 / p. 575-582 : ill https://ieeexplore.ieee.org/document/6037463

Software-based self-test for microprocessors with high-level decision diagrams = Mikroprotsessorite tarkvara-põhine enesetestimine kõrgtasandi otsustusdiagrammide põhjal
Jasnetski, Artjom 2018 https://digi.lib.ttu.ee/i/?10629 https://www.ester.ee/record=b5151486*est

Software-based self-test generation for microprocessors with high-level decision diagrams
Ubar, Raimund-Johannes; **Tšertov, Anton**; **Jasnetski, Artjom**; **Brik, Marina** LATW2014 : 15th IEEE Latin-American Test Workshop : Fortaleza, Brazil, March 12th-15th, 2014 2014 / [6] p. : ill

Software-based self-test generation for microprocessors with high-level decision diagrams
Jasnetski, Artjom; **Ubar, Raimund-Johannes**; **Tšertov, Anton**; **Brik, Marina** Proceedings of the Estonian Academy of Sciences 2014 / p. 48-61 : ill https://artiklid.elnet.ee/record=b2665215*est https://doi.org/10.3176/proc.2014.1.08 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Software-based self-test with decision diagrams for microprocessors
Ubar, Raimund-Johannes; Jasnetski, Artjom; **Tšertov, Anton**; Oyeniran, Adeboye Stephen 2018

SPICE-inspired fast gate-level computation of NBTI-induced delays in nanoscale logic
Kostin, Sergei; **Raik, Jaan**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 2015 IEEE 18th International Symposium on Design and Diagnostics of Electronic Circuits & Systems DDECS 2015 : 22-24 April 2015, Belgrade, Serbia : proceedings 2015 / p. 223-228 : ill

SSBDD model : advantageous properties and efficient simulation algorithms
Raik, Jaan; **Jutman, Artur**; **Ubar, Raimund-Johannes** ETW'02 : 7th IEEE European Test Workshop, Gorfu Greece, May 26-29, 2002 : informal digest 2002 / p. 345-346 : ill

SSBDDs : advantageous model and efficient algorithms for digital circuit modeling, simulation & test
Jutman, Artur; **Raik, Jaan**; **Ubar, Raimund-Johannes** 5th International Workshop on Boolean Problems : September 19-20, 2002,Freiberg (Sachsen) : proceedings 2002 / p. 157-166 : ill

SSBDDs and double topology for multiple fault reasoning
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** Proceedings of IEEE East-West Design & Test Symposium

(EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 23-28 https://www.semanticscholar.org/paper/SSBDDs-and-Double-Topology-for-Multiple-Fault-Ubar-Kostin/8ba04611a41768f0c277a4ba46ca666132fc2f65

Structural decision diagrams in digital test : theory and applications
Ubar, Raimund-Johannes; **Raik, Jaan**; **Jenihhin, Maksim**; **Jutman, Artur** 2024 https://doi.org/10.1007/978-3-031-44734-1 https://www.ester.ee/record=b5734441*est

Structural fault collapsing by superposition of BDDs for test generation in digital circuits
Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Raik, Jaan**; **Jutman, Artur** Proceedings of the Eleventh International Symposium on Quality Electronic Design ISQED 2010 : March 22-24, 2010 San Jose, California USA 2010 / p. 250-257 : ill https://ieeexplore.ieee.org/document/5450451

Structurally synthesized binary decision diagrams
Jutman, Artur; Peder, Ahti; **Raik, Jaan**; Tombak, Mati; **Ubar, Raimund-Johannes** Boolean Problems : 6th International Workshop : September 23-24, 2004, Freiberg 2004 / p. 271-278 : ill

Structurally synthesized multiple input BDDs for simulation of digital circuits
Ubar, Raimund-Johannes; **Mironov, Dmitri**; **Raik, Jaan**; **Jutman, Artur** 16th IEEE International Conference on Electronics, Circuits, and Systems, ICECS 2009 : Yasmine Hammamet, Tunesia, 13-19 December, 2009 2009 / p. 451-454 : ill http://dx.doi.org/10.1109/ICECS.2009.5410895

Structurally synthesized multiple input BDDs for speeding up logic-level simulation of digital circuits
Mironov, Dmitri; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 13th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : DSD 2010 : Lille, France, 1-3 September 2010 : proceedings 2010 / p. 658-663 : ill https://ieeexplore.ieee.org/document/5615526

Success story of the Computer Engineering Department at the Tallinn University of Technology in EU projects
Ubar, Raimund-Johannes; **Kruus, Margus** The parliament magazine : European politics and policy 2006 / p. 33 : ill

Suure eksperimendi ootel
Ubar, Raimund-Johannes Tehnikaülikool 1998 / 19. jaan., lk. 1, 3 https://www.ester.ee/record=b5309277*est

Sünergiline teaduskeskus : Integreeritud elektroonikasüsteemide ja biomeditsiinitehnika tippkeskus CEBE
Ubar, Raimund-Johannes Mente et Manu 2011 / lk. 2, 5 : portr https://www.ester.ee/record=b1242496*est

Sünkroonsete järjestiklülituste testide deduktiivse analüüsi meetod
Evartson, Teet; **Ubar, Raimund-Johannes** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 42 https://www.ester.ee/record=b2449987*est

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation
Leveugle, R.; **Ubar, Raimund-Johannes** Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358 https://hal.science/ccsd-00015077/

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation
Leveugle, R.; **Ubar, Raimund-Johannes** Electron technology 1999 / 3, p. 282-287 : ill

Synthesis of high-level decision diagrams for functional test pattern generation
Ubar, Raimund-Johannes; **Raik, Jaan**; **Karputkin, Anton**; **Tombak, Mati** Proceedings of the 16th International Conference Mixed Design of Integrated Circuits and Systems MIXDES 2009 : Lodz, Poland, 25-27 June, 2009 2009 / p. 519-524 : ill

Synthesis of multiple fault oriented test groups from single fault test sets [Electronic resource]
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Raik, Jaan** 2013 8th International Conference on Design & Technology of Integrated Systems in Nanoscale Era (DTIS) : 26-28 March 2013, Abu Dhabi, UAE 2013 / p. 36-41 : ill [CD-ROM]

A system for teaching basic and advanced topics of IEEE 1149.1 boundary scan standard (extended abstract)
Jutman, Artur; Rosin, Vjatšeslav; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Proceedings of 16th EAEEIE Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Lappeenranta, Finland, 6th-8th June 2005 2005 / [2] p. : ill

System modeling for processor-centric test automation = Süsteemide modelleerimine protsessorikesksete testprogrammide sünteesi automatiseerimiseks
Tšertov, Anton 2012 https://www.ester.ee/record=b2751131*est

Targeting conditional operations in sequential test pattern generation
Raik, Jaan; **Ubar, Raimund-Johannes** 9th European Test Symposium : ETS'04 : Congress Center, Ajaccio, Corsica, France,May 23-26, 2004 2004 / p. 17-18 : ill

https://www.researchgate.net/publication/239717327_Targeting_Conditional_Operations_in_Sequential_Test_Pattern_Generation

Teaching advanced test issues in digital electronics
Ubar, Raimund-Johannes; **Orasson, Elmet**; **Raik, Jaan**; Wuttke, Heinz-Dietrich Proceedings of the 6th IEEE International Conference on Information Technology Based Higher Education and Training : ITHET : July 7-9, 2005, Juan Dolio, Dominican Republic 2005 / p. S2B-1 - S2B-6 : ill http://dx.doi.org/10.1109/ITHET.2005.1560318

Teaching dependability issues in system engineering at the Technical University of Tallinn
Ubar, Raimund-Johannes 90th Anniversary Jubilee Seminar on Engineering Education, University of Wismar, Germany, May 6-8, 1998 : preprints of proceedings 1998 / p. 1-5 (invited paper)

Teaching dependability issues in systems engineering at the Technical University of Tallinn
Ubar, Raimund-Johannes Global journal of engineering education 1998 / 2, p. 215-218

Teaching diagnostic modeling of digital systems with decision diagrams [Electronic resource]
Ubar, Raimund-Johannes; **Raik, Jaan**; **Mironov, Dmitri**; **Evartson, Teet**; **Orasson, Elmet**; **Aarna, Margit**; Wuttke, Heinz-Dietrich Proceedings of 12th IASTED International Conference on Computers and Advanced Technology in Education - CATE 2009 : St.Thomas, US, November 22-24, 2009 2009 / p. 1-6. [CD-ROM]

Teaching digital RT-level self-test using a Java applet
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 322-328 : ill

Teaching digital system test
Oyeniran, Adeboye Stephen; **Ubar, Raimund-Johannes**; **Kruus, Margus** The 27th EAEEIE Annual Conference : June 7-9, 2017, Grenoble 2017 / [6] p

Teaching digital test with BIST analyzer
Jutman, Artur; **Tšertov, Anton**; **Tšepurov, Anton**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 123-128 : ill http://dx.doi.org/10.1109/EAEEIE.2008.4610171

Teaching research in the laboratory using diagnosis environment for digital systems
Kostin, Sergei; **Ubar, Raimund-Johannes**; **Raik, Jaan**; **Aarna, Margit**; **Brik, Marina**; Wuttke, Heinz-Dietrich 2009 EAEEIE annual conference : 20th Annual Conference of the European Association for Education in Electrical and Information Engineering : Valencia, Spain, June 22-24, 2009 2009 / p. 280-283 https://ieeexplore.ieee.org/document/5335462

Teaching test and design for testability with TURBO-TESTER software
Jervan, Gert; **Markus, Antti**; **Paomets, Priidu**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 3rd Workshop on Mixed Design of Integrated Circuits and Systems, Lodz, May 1996 1996 / p. 589-594

Teadus hämaratel kõrvaltänavatel
Ubar, Raimund-Johannes Postimees 1998 / 14. märts, lk. 7

Teadus ja tehnika ebalevas Eestis : [vestlusring]
Ubar, Raimund-Johannes; **Engelbrecht, Jüri**; **Mägi, Vahur** Tehnika ja Tootmine 1995 / 1, lk. 33-37

Teaduse mitmekesisus on riigi rikkus : [vestlusringis Jüri Engelbrecht, Raimund Ubar ja Jüri Kivimäe]
Engelbrecht, Jüri; **Ubar, Raimund-Johannes**; Kivimäe, Jüri; Jõgi, Mall Kultuurileht 1994 / 2. dets., lk. 6-7: ill

Teaduse mõõtmisest, hindamisest ja auhindamisest
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2007 2008 / lk. 17-24

Teadusemees. Mälestused
Ubar, Raimund-Johannes; Põldre, Jüri 2011 https://www.ester.ee/record=b2739593*est

Teaduses sünnivad maailmarekordid
Ubar, Raimund-Johannes Eesti Päevaleht 1998 / 28. jaan., lk. 10

Teadusfondi Nõukogu teiselt esimehelt (1993-96)
Ubar, Raimund-Johannes Ülevaade Eesti Teadusfondi tegevusest 1990-96 1996 / lk. 24

Teaduspreemia laureaadi sõnavõtt : [teaduspreemiate üleandmisel]
Ubar, Raimund-Johannes Eesti Vabariigi preemiad 2016 : teadus. F. J. Wiedemanni keeleauhind. Kultuur. Sport 2016 / lk. 20-21

Teaduspreemia pikaajalise tulemusliku teadus- ja arendustöö eest : Raimund Ubar
Ubar, Raimund-Johannes Eesti Vabariigi preemiad 2016 : teadus. F. J. Wiedemanni keeleauhind. Kultuur. Sport 2016 / lk. 34-61 : fot., portr

Teaduspreemia tehnikateaduste alal töö "Uued meetodid digitaalsüsteemide disaini ja diagnostika valdkonnas" eest
Ubar, Raimund-Johannes Eesti Vabariigi teaduspreemiad 1999 1999 / lk. 24-31

Teaduspõhisus eesriide taga
Ubar, Raimund-Johannes Teadus ja ühiskond 2018 / lk. 9-27 : ill., fot

Tehissüsteemide veakindlusest : [TTÜ arvutitehnika instituudi teadustöödest]
Ubar, Raimund-Johannes Horisont 2006 / 2, lk. 64-69 : ill https://artiklid.elnet.ee/record=b2039558*est

Tehnikateaduste ekspertkomisjon
Ubar, Raimund-Johannes Ülevaade Eesti Teadusfondi tegevusest 1990-96 1996 / lk. 38-44 : ill., portr

Tehnikateaduste tee Eestis
Ubar, Raimund-Johannes Eesti tulevikusuundumused 1994 / lk. 27-38

Tehnikateaduste tee Eestis : ettekanne Eesti Teadlaste Liidu sümpoosionil "Eesti tulevikusuundumused" 14. aprillil 1994 TTÜs
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 1994 1995 / lk. 127-140

Tehnikaülikool Eurochip'i liikmeks
Ubar, Raimund-Johannes Õhtuleht 1993 / 5. märts, lk. 8: ill

Tehnikaülikoolis tegutseb elektroonika kompetentsuskeskus
Ubar, Raimund-Johannes Eesti Päevaleht 1995 / 13. nov

Tehnokultuuri võimalikkusest tänases Eestis
Ubar, Raimund-Johannes Kultuurileht 1994 / 6., 13. mai, lk. 6 https://artiklid.elnet.ee/record=b1886371*est

Tehnoloogia usaldamisest
Ubar, Raimund-Johannes Horisont 2011 / 5, lk. 10-19 : ill https://artiklid.elnet.ee/record=b2427737*est

Temporally extended high-level decision diagrams for PSL assertions simulation
Jenihhin, Maksim; **Raik, Jaan**; **Tšepurov, Anton**; **Ubar, Raimund-Johannes** Proceedings : Thirteenth IEEE European Test Symposium : ETS 2008 : 25-29 May 2008, Verbania, Italy 2008 / p. 61-68 : ill https://ieeexplore.ieee.org/document/4556029

10th IEEE European Test Symposium
Ubar, Raimund-Johannes; Prinetto, Paolo; **Raik, Jaan** IEEE journal of design & test of computers 2005 / p. 480-481 : phot http://dx.doi.org/10.1109/MDT.2005.106

"Tervis ruudus", ehk, Tippkeskuse CEBE lugu
Ubar, Raimund-Johannes Teadusmõte Eestis (X). Tehnikateadused. 3 : [artiklikogumik] 2019 / lk. 200-215 : ill., fot https://www.ester.ee/record=b5208765*est

Test configurations for diagnosing faulty links in NoC switches
Raik, Jaan; **Ubar, Raimund-Johannes**; **Govind, Vineeth** 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 29-34 : ill http://dx.doi.org/10.1109/ETS.2007.41

Test configurations for diagnosing faulty links in NoC switches
Raik, Jaan; **Ubar, Raimund-Johannes**; **Govind, Vineeth** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 33-37 : ill

Test cost minimization for hybrid BIST
Jervan, Gert; Peng, Zebo; **Ubar, Raimund-Johannes** IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 25-27 October 2000, Yamanashi, Japan : proceedings 2000 / p. 283-298 : ill https://ieeexplore.ieee.org/abstract/document/887168

Test cover calculation in digital systems with word-level decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Ivask, Eero**; **Brik, Marina** Вестник Томского государственного университета 2002 / с. 315-319 : ил

Test generation : a hierarchical approach

Jervan, Gert; **Ubar, Raimund-Johannes**; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 67-81 : ill

Test generation for digital systems
Ubar, Raimund-Johannes Digest of papers - FTCS 13th Annual International Symposium on Fault-Tolerant Computing, June 28 - 30, 1983, Milano, Italy 1983 / p. 374-377

Test generation for digital systems at functional level
Ubar, Raimund-Johannes; Kuchcinski, Ktzysztof; Peng, Z. Research report LiTH-IDA-R-90-06, Linköping University, Sweden 1990 / p. 1-21

Test generation for digital systems based on alternative graphs
Ubar, Raimund-Johannes Dependable Computing - EDCC-1 : First European Dependable Computing Conference, Berlin, Germany, October 1994 : proceedings 1994 / p. 151-164: ill

Test generation for finite state machines
Ubar, Raimund-Johannes; **Brik, Marina** BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 233-236: ill

Test generation for microprocessor control mechanisms
Lohuaru, Tõnu; **Ubar, Raimund-Johannes** FTSD-10 : Deseta Mezdunarodnaja Konferencija "Nadezdnost i Diagnostika na ECM. Mikrokompjutri i Sistemi", Varna, Bulgaria, 1987 = 10th International Conference on Fault-Tolerant Systems and Diagnostics (1987) 1987 / p. 305-311

Test generation for microprocessors on alternative graphs
Alango, Villem; **Kont, Toomas**; **Ubar, Raimund-Johannes** 33. Internationales Wissenschaftliches Kolloquium : 24.-28.10.1988. H.3 Vortragsreihe B, technische und angewandte Informatik/Computertechnik 1988 / p. 11-14

Test generation techniques and algorithms
Ubar, Raimund-Johannes; Gramatova, Elena; Fisherova, Maria Handbook of testing electronic systems 2005 / p. 99-173 : ill

Test generation with structurally synthesized BDD models
Raik, Jaan; **Ubar, Raimund-Johannes** Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 66-68

Test methods for crosstalk-induced delay and glitch faults in network-on-chip interconnects implementing asynchronous communication protocols
Bengtsson, Tomas; Kumar, Shashi; **Ubar, Raimund-Johannes**; **Jutman, Artur**; Peng, Zebo IET computers and digital techniques 2008 / 6, p. 445-460 https://www.diva-portal.org/smash/record.jsf?dswid=-5073&aq2=%5B%5B%5D%5D&c=39&af=%5B%5D&searchType=SIMPLE&sortOrder2=title_sort_asc&language=en&pid=diva2%3A290043&aq=%5B%5B%7B%22personId%22%3A%22authority-person%3A23389%22%7D%5D%5D&sf=all&aqe=%5B%5D&sortOrder=author_sort_asc&onlyFullText=false&noOfRows=50

Test pattern generation for microprocessor systems on the alternative graph model
Ubar, Raimund-Johannes Proceedings of the 3rd Symposium of the IMEKO Technical Committee on Technical Diagnostics (TC10), held in Moscow, October 3 - 5, 1983 1985 / p. 403-410

Test set minimization using bipartite graphs
Markus, Antti; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 175-178: ill

Test synthesis with alternative graphs
Ubar, Raimund-Johannes IEEE design & test of computers 1996 / Spring, p. 48-57: ill

Test system for fault detection and diagnosis in microprocessor control devices
Ubar, Raimund-Johannes; Lohuaru, Tõnu; Männisalu, Mati; Pukk, P.; Vanamölder, E. Tallinna Tehnikaülikooli Toimetised 1990 / lk. 63-77: ill

Test time minimization for hybrid BIST of core-based systems
Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** Journal of computer science and technology 2006 / 6, p. 907-912 : ill https://link.springer.com/article/10.1007/s11390-006-0907-x

Test time minimization for hybrid BIST of core-based systems
Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** 12th Asian Test Symposium (ATS 2003) : 17-19 November 2003, Xian, China 2003 / p. 318-325 : ill https://link.springer.com/article/10.1007/s11390-006-0907-x

Test time minimization for hybrid BIST with test pattern broadcasting
Ubar, Raimund-Johannes; Jenihhin, Maksim; **Jervan, Gert**; Peng, Zebo IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 112-116 : ill https://www.ida.liu.se/labs/eslab/publications/pap/db/norchip03.pdf

Testability analysis for efficient register-transfer level test generation [Electronic resource]
Nõmmeots, Tanel; **Raik, Jaan**; **Ubar, Raimund-Johannes** 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [4] p. [CD-ROM]

Testability calculation for digital circuits with decision diagrams
Ubar, Raimund-Johannes 3rd IEEE Latin American Test Workshop : LATW'02, Montevideu, Uruguay, February 10-13, 2002 : digest of papers 2002 / p. 137-143 : ill https://dblp.org/rec/conf/latw/Ubar02.html

Testability guided hierarchical test generation with decision diagrams
Ubar, Raimund-Johannes; **Raik, Jaan**; **Nõmmeots, Tanel** 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 265-271 https://www.semanticscholar.org/paper/Testability-Guided-Hierarchical-Test-Generation-Ubar-Raik/c6301ac35d003c92f3867f26e2e75b87e1ad9b47

Testentwicklung für Mikroprozessorsystem mit Hilfe der alternativen Graphen
Alango, Villem; **Kont, Toomas**; **Ubar, Raimund-Johannes** 33. Internationales wissenschaftliches Kolloquium : 24.-28.10.1988. H.1. 1988 / S- 11-14 https://www.ester.ee/record=b2936968*est

Testide genereerimine loogikalülituste alternatiivsete graafide süsteemi mudeli abil
Saarma, G.; **Ubar, Raimund-Johannes** XXIX vabariiklik üliõpilaste teaduslik- tehniline konverents 30. märtsist - 1. aprillini 1977 : ettekannete teesid 1977 / lk. 43 https://www.ester.ee/record=b2449987*est

Testing of systems using software
Ubar, Raimund-Johannes Concise encyclopedia of software engineering 1993 / p. 352-356

Testing strategies for networks on chip
Ubar, Raimund-Johannes; **Raik, Jaan** Networks on chip 2003 / p. 131-152 : ill https://link.springer.com/chapter/10.1007/0-306-48727-6_7

Testing tools for training and education
Balaž, M.; **Jutman, Artur**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 12th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2005 : Krakow, Poland, 22-25 June, 2005. Vol. 1 of 2 2005 / p. 671-676 : ill

The dildis-project-using applets for more demonstrative lectures in digital systems design and test
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich FIE 2001 : 31st Annual Frontiers in Educations Conference : Impact on Engineering and Science Education : Reno, Nevada, October 10-13, 2001 : conference program 2001 / p. 83 https://ieeexplore.ieee.org/document/963996

The dildis-project-using applets for more demonstrative lectures in digital systems design and test
Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the 31st ASEE/IEEE Frontiers in Educations Conference : FIE'2001 : Reno, Nevada 2001 / p. SIE-2-7 https://ieeexplore.ieee.org/document/963996

The synthesis level in Bloom's taxonomy - a nightmare for an LMS
Wuttke, Heinz-Dietrich; **Ubar, Raimund-Johannes**; Henke, Karsten; **Jutman, Artur** 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 199-204 : ill http://dx.doi.org/10.1109/EAEEIE.2008.4610186

3D parallel fault simulation
Gorev, Maksim; **Ubar, Raimund-Johannes** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 39-42 : ill

Timing simulation of digital circuits with binary decision diagrams
Ubar, Raimund-Johannes; **Jutman, Artur**; Peng, Z. Design, Automation and Test in Europe : Conference and Exhibition 2001 : Munich, Germany, March 13-16, 2001 : proceedings 2001 / p. 460-466 : ill https://ieeexplore.ieee.org/document/915063

Timing-critical path analysis with structurally synthesized BDDs
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Jenihhin, Maksim**; **Raik, Jaan**; **Olugbenga, Niyi-Leigh**; **Viies, Vladimir** 2018 7th Mediterranean Conference on Embedded Computing (MECO) 2018 / 6 p. : ill https://doi.org/10.1109/MECO.2018.8406051

Tippteadus ja ülikool
Ubar, Raimund-Johannes Mente et Manu 2014 / lk. 11-15 : fot https://artiklid.elnet.ee/record=b2705056*est

Tippteadus ja ülikool
Ubar, Raimund-Johannes Teadusmõte Eestis (VIII). Teaduskultuur : [artiklikogumik] 2013 / lk. 46-53 : portr

Tollimaks tegi õpperaamatu hirmkalliks
Ubar, Raimund-Johannes Eesti Päevaleht 1999 / 6. dets., lk. 2

A tool for random test generation targeting high diagnostic resolution
Osimiry, Emmanuel Ovie; **Kostin, Sergei**; **Raik, Jaan**; **Ubar, Raimund-Johannes** BEC 2016 : 2016 15th Biennial Baltic Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-5, 2016, Tallinn, Estonia 2016 / p. 79-82 : ill http://www.ester.ee/record=b2150914*est

A tool for teaching hierarchical fault diagnosis in digital circuits
Ubar, Raimund-Johannes; **Kostin, Sergei**; **Orasson, Elmet**; **Evartson, Teet**; **Brik, Marina** Proceedings of 9th European Workshop on Microelectronics Education – EWME'12 : Grenoble, France, May 9-11, 2012 2012 / p. 1-4

A tool set for teaching design-for-testability of digital circuits
Kostin, Sergei; **Orasson, Elmet**; **Ubar, Raimund-Johannes** EWME 2016 : 11th European Workshop on Microelectronics Education : May 11-13, 2016, Southampton, UK 2016 / [6] p. : ill https://doi.org/10.1109/EWME.2016.7496466

Topological analysis of SSBDDs with applications in fault diagnosis
Ubar, Raimund-Johannes Proceedings of 10th International Workshop on Boolean Problems : Freiberg, Germany, September 19-21, 2012 2012 / p. 1-16

Towards artificial intelligence based automatic adaptive response analyzer for high frequency analog BIST
Petlenkov, Eduard; **Jutman, Artur**; **Nõmm, Sven**; **Ubar, Raimund-Johannes** CIMSA 2008 : IEEE International Conference on Computational Intelligence for Measurement Systems and Applications : Istanbul, Turky, July 14-16, 2008 2008 / p. 99-104 : ill https://ieeexplore.ieee.org/document/4595841

Trainer 1149: a boundary scan simulation bundle for labs
Jutman, Artur; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; Shibin, Konstantin; Rosin, Vjatšeslav MIXDES 2011 : 18th International Conference "Mixed Design of Integrated Circuits and Systems" : June 16-18, 2011, Gliwice, Poland 2011 / p. 520-525

Transition delay fault simulation with parallel critical path back-tracing and 7-valued algebra
Kõusaar, Jaak; **Ubar, Raimund-Johannes**; **Devadze, Sergei**; **Raik, Jaan** Microprocessors and microsystems 2015 / p. 1130-1138 : ill https://doi.org/10.1016/j.micpro.2015.05.003 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

True path tracing in structurally synthesized BDDs for testability analysis of digital circuits
Ubar, Raimund-Johannes; **Jürimägi, Lembit**; **Oyeniran, Adeboye Stephen**; **Jenihhin, Maksim** Euromicro Conference on Digital System Design : DSD 2019 : 28 - 30 August 2019 Kallithea, Chalkidiki, Greece : proceedings 2019 / p. 492-499 : ill https://doi.org/10.1109/DSD.2019.00077

Tsivilisatsioon ei tea, kuhu ta edasi tormab
Ubar, Raimund-Johannes Tallinna Ülikoolid 1998 / 3, lk. 21-23: ill

Turbo tester - diagnostic package for research and training
Aarna, Margit; **Ivask, Eero**; **Jutman, Artur**; **Orasson, Elmet**; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Vislogubov, Vladislav; Wuttke, Heinz-Dietrich Radioelectronics and informatics 2003 / p. 69-73 : ill

Turbo tester : a CAD system for teaching digital test
Jervan, Gert; **Markus, Antti**; **Paomets, Priidu**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Microelectronics education : proceedings of the 2nd European Workshop held in Noordwijkerhout, The Netherlands, 14-15 May 1998 1998 / p. 287-290: ill https://link.springer.com/chapter/10.1007/978-94-011-5110-8_66

Turbo Tester : a low cost PC-based CAD system for training digital test
Ubar, Raimund-Johannes SampTA'95 : 1995 Workshop on Sampling Theory & Applications, Jurmala, Latvia, September 20-22, 1995 1995

TURBO TESTER : a set of software tools for CAD of test for digital circuits
Ubar, Raimund-Johannes; **Tulit, Viljar**; **Buldas, Ahto**; **Saarepera, Märt** Fourth EUROCHIP Workshop on VLSI Design Training, 29 September to 1 October 1993, [Toledo] 1993 / p. 396

Turning JTAG inside out for fast extended test access
Devadze, Sergei; **Jutman, Artur**; **Aleksejev, Igor**; **Ubar, Raimund-Johannes** 10th IEEE Latin American Test Workshop : 2-5 March 2009, Brazil 2009 / [6] p. : ill https://ieeexplore.ieee.org/document/4813799

Two-level simulation-based test generation for finite state machines
Brik, Marina; **Ubar, Raimund-Johannes** 17th NORCHIP Conference : Oslo, Norway, 8-9 November 1999 : proceedings 1999 / p.

211-216: ill

Tõe haprusest teaduse ja ühiskonna dialoogis
Ubar, Raimund-Johannes Eesti Teaduste Akadeemia aastaraamat = Annales academiae scientarum Estonicae 2017 2018 / lk. 51-53 https://www.ester.ee/record=b1218094*est

Tõe haprusest teaduse ja ühiskonna dialoogis
Ubar, Raimund-Johannes Postimees 2017 / AK : arvamus, kultuur, lk. 7 https://teadus.postimees.ee/3997875/raimund-ubar-toe-haprusest-teaduse-ja-uhiskonna-dialoogis

Ultra fast parallel fault analysis on structurally synthesized BDDs
Ubar, Raimund-Johannes; **Devadze, Sergei**; **Raik, Jaan**; **Jutman, Artur** 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 131-136 : ill http://dx.doi.org/10.1109/ETS.2007.43

Understanding boundary scan test with Trainer 1149
Jutman, Artur; **Devadze, Sergei**; **Shibin, Konstantin**; Rosin, Vjatšeslav; **Ubar, Raimund-Johannes** 22nd EAEEIE annual conference : June, 13-15, 2011, Maribor, Slovenija : conference book 2011 / p. 21-22 https://ieeexplore.ieee.org/document/6165727

Untestable fault identification in sequential circuits using model-checking
Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes**; **Krivenko, Anna** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 257-262 : ill https://ieeexplore.ieee.org/document/4711554

Untestable fault identification in sequential circuits using model-checking
Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes**; **Krivenko, Anna** Proceedings of the 17th Asian Test Symposium ATS 2008 : November 24-27, 2008, Sapporo, Japan 2008 / p. 21-26 : ill http://dx.doi.org/10.1109/ATS.2008.22

Using Tabu Search for optimization of memory-constrained hybrid BIST
Kruus, Helena; **Jervan, Gert**; **Ubar, Raimund-Johannes** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 155-158 : ill

Using Tabu Search for optimization of memory-constrained hybrid BIST
Kruus, Helena; **Jervan, Gert**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 85-88 : ill

Using Tabu search method for optimizing the cost of hybrid BIST
Kruus, Helena; **Ubar, Raimund-Johannes**; **Jervan, Gert**; Peng, Z. XVI Conference on Design of Circuits and Integrated Systems : Porto, Portugal, 2001 2001 / p. 445-450 https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=e97bb394ff71aa0affcc5fb372404bbc246888a8

Uued meetodid digitaalsüsteemide disaini ja diagnostika valdkonnas : kommentaar Eesti Vabariigi teaduse aastapreemia pälvinud tööle
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 1998 1999 / lk. 142-145

Uurimistoetuse juhend ja vormid
Ubar, Raimund-Johannes 1995 https://www.ester.ee/record=b1067614*est

Vaba semester Prantsusmaal
Ubar, Raimund-Johannes Tehnikaülikool 1998 / 19. veebr., lk. 6-7; 9. märts, lk. 8-9; 23. märts, lk. 6-7; 13. apr., lk. 6-7; 27. apr., lk. 4-5; 11. mai, lk. 4-5 https://artiklid.elnet.ee/record=b2326039*est

Vahespurt nanomeeterdistantsil
Ubar, Raimund-Johannes Õpetajate Leht 2011 / lk. 7 : portr https://artiklid.elnet.ee/record=b2408293*est

Valik arvamusi läbi aastate : [arvamused ka TTÜga seotud akadeemikutelt: Rein Küttner, Anto Raukas, Mart Saarma, Boris Tamm, Enn Tõugu, Raimund-Johannes Ubar]
Küttner, Rein; **Raukas, Anto**; **Saarma, Mart**; **Tamm, Boris, inform.**; **Tõugu, Enn**; **Ubar, Raimund-Johannes** Akadeemia 2008 / lk. 2153-2188, 2327-2328 https://artiklid.elnet.ee/record=b1998916*est https://www.ester.ee/record=b1071914*est

Vastab tehnikateadlane Raimund-Johannes Ubar : intervjuu
Ubar, Raimund-Johannes Horisont 1993 / 6, lk. 32-33 : portr

Web based tools for synthesis and testing of digital devices
Devadze, Sergei; **Jutman, Artur**; **Kruus, Margus**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** Proceedings of the International Conference on Computer Systems and Technologies (e-Learning) : CompSysTech'2002, Sofia, Bulgaria, 20-21 June 2002 / p. 1.9-1 - 1.9-6 : ill

https://www.researchgate.net/publication/250738271_Web_Based_Tools_for_Synthesis_and_Testing_of_Digital_Devices

Web-based applet for teaching boundary scan standard IEEE 1149.1
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 584-589 : ill
https://www.semanticscholar.org/paper/WEB-BASED-APPLET-FOR-TEACHING-BOUNDARY-SCAN-IEEE-.-J.-Utman/3bd1b47848612e44772b4c84a2913c419de940fa

Web-based environment for digital electronics test tools
Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes**; Schneider, Andre Virtual Enterprises and collaborative networks : IFIP 18th World Computer Congress [and] TC5/WG5.5 - 5th Working Conference on Virtual Enterprises : 22-27 August 2004, Toulouse, France 2004 / p. 435-442 : ill https://link.springer.com/chapter/10.1007/1-4020-8139-1_46

Web-based framework for distributed remote laboratory in the field of digital system test
Ivask, Eero; **Jutman, Artur**; **Raik, Jaan**; **Ubar, Raimund-Johannes** 19th EAEEIE Annual Conference : June 29-July 2, 2008, Tallinn, Estonia : formal proceedings 2008 / p. 182-187 : ill http://dx.doi.org/10.1109/EAEEIE.2008.4610183

Web-based framework for parallel distributed test [Electronic resource]
Ivask, Eero; **Raik, Jaan**; **Ubar, Raimund-Johannes** 2008 IEEE Design and Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 271-274 : ill. [CD-ROM] https://ieeexplore.ieee.org/document/4538800

Web-based software package for e-learning and research training in digital system design
Jutman, Artur; **Kruus, Margus**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes**; Wuttke, Heinz-Dietrich Информационные технологии в науке, образовании, телекоммуникации и бизнесе : Материалы XXXII Международной конференции IT+SE'2005 : Украина, Крым, Ялта-Гурзуф, 19-28 мая 2005 г 2005 / [2] p

Web-based training system for teaching basics of RT-level digital design, test, and design for test [Electronic resource]
Devadze, Sergei; **Jutman, Artur**; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [6] p. : ill. [CD-ROM]

Web-based training system for teaching principles of boundary scan technique
Jutman, Artur; **Sudnitsõn, Aleksander**; **Ubar, Raimund-Johannes** Proceedings of the 14th EAEEIE Annual International Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Gdansk, Poland, 2003 2003 / p. 1-6 : ill

Vector decision diagrams for simulation of digital systems
Ubar, Raimund-Johannes; Morawiec, Adam; **Raik, Jaan** DDECS'2000 2000 / p. 44-51

Vektorielle alternative graphen und Fehlerdiagnose für digitale Systeme
Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftlishe Zeitschrift für die gesamte elektronische Nachrichtentechnik 1981 / p. 25-28 : ill https://www.ester.ee/record=b1550811*est

VHDL based test generation system
Jervan, Gert; **Markus, Antti**; **Raik, Jaan**; **Ubar, Raimund-Johannes** Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 145-148

VILAB test generation tools running under the MOSCITO system
Schneider, Andre; **Ivask, Eero**; **Raik, Jaan**; **Ubar, Raimund-Johannes** VILAB User Forum : Györ, Hungary, 2001 2001 / [12] p

Virtuaalse labori lugu : (case story)
Ubar, Raimund-Johannes Tehnikaülikool 1998 / 31. aug., lk. 2-3 https://artiklid.elnet.ee/record=b2326044*est

Virtual laboratory for research in dependable microelectronics
Diener, Karl-Heinz; Elst, G.; Gramatova, Elena; Kuzmicz, W.; Peng, Z.; **Ubar, Raimund-Johannes** The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 217-220 : ill

Virtual Research & Development Laboratory : a European project
Ubar, Raimund-Johannes Electronics Design and Test : international user forum : compendium of papers : Tallinn Technical University, 11. October 2000, Estonia 2000 / [14] p. : ill https://artiklid.elnet.ee/record=b2326049*est

Über einige Probleme der Testsatzanalyse für digitale Systeme
Ubar, Raimund-Johannes Nachrichtentechnik, Elektronik : technisch-wissenschaftlishe Zeitschrift für die gesamte elektronische Nachrichtentechnik 1977 / p. 149-150 https://www.ester.ee/record=b1550811*est

Über einige Probleme der Testsatzanalyse für digitale Systeme
Ubar, Raimund-Johannes Wissenschaftliche Zeitschrift 1976 / p. 447-449 https://www.ester.ee/record=b1516616*est

Ühest kirjutamata jäänud aruandest ehk kes koordineeriks ülikoolis interdistsiplinaarsust
Ubar, Raimund-Johannes Tehnikaülikool 1997 / 18. dets., lk. 4-6: ill

Ülemiste vanakesest Toompeal
Ubar, Raimund-Johannes Postimees 1993 / 11. mai, lk. 2: portr https://artiklid.elnet.ee/record=b1915312*est

Ülevaade Eesti Teadusfondi tegevusest 1990-96
Martinson, Helle; **Ubar, Raimund-Johannes** 1996 https://www.ester.ee/record=b1058570*est

Ülikooli aknad on õhtuti pimedad, sest kõik ei suuda olla Diogenesed : [kõne doktorite promoveerimisaktusel TTÜ 75. aastapäeval]
Ubar, Raimund-Johannes Tehnikaülikool 1993 / 19. okt., lk. 2-3: portr

Ülikoolid akadeemilise kapitalismi tõmbetuules
Ubar, Raimund-Johannes Akadeemia 2002 / 4, lk. 675-690

Ülikoolid akadeemilise kapitalismi tõmbetuules : akadeemiline loeng 17. detsembril 2001 TTÜs
Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2001 2003 / lk. 328-339

Ülikoolide saatusest teabeühiskonnas
Ubar, Raimund-Johannes Postimees 1997 / 24. mai, lk. 7

Автоматизация проектирования в электронике - система SPADE
1982 https://www.ester.ee/record=b1312243*est https://digikogu.taltech.ee/et/Item/4bb3c838-273f-4f66-907d-fe44df0c246b

Автоматический синтез тестов для диагностики цифровых устройств
Lohuaru, Tõnu; Pall, Martin; **Ubar, Raimund-Johannes** Eesti NSV Teaduste Akadeemia toimetised. Füüsika. Matemaatika = Известия Академии наук Эстонской ССР. Физика. Математика = Proceedings of Academy of Sciences of the Estonian SSR. Physics. Mathematics 1983 / lk. 84-94 https://www.ester.ee/record=b1264310*est

Алгоритм генерирования тестов для комбинационных логических схем
Pall, I.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 133 https://www.ester.ee/record=b1306141*est

Альтернативные графы и техническая диагностика дискретных объектов
Ubar, Raimund-Johannes Электронная техника. Серия 8, Управление качеством и стандартизация : научно-технический сборник 1988 / с. 33-57

Анализ диагностических тестов для комбинационных цифровых схем методом обратного прослеживания неисправностей
Ubar, Raimund-Johannes Автоматика и телемеханика 1977 / с. 168-176 https://www.ester.ee/record=b1515055*est

Вероятностное тестирование цифровых схем и альтернативные графы
Ubar, Raimund-Johannes Машинное проектирование электронных устройств и систем 1989 / с. 89-96

Генерирование групповых тестов для цифровых схем на модели альтернативных графов
Kivi, E.; **Ubar, Raimund-Johannes** Тезисы докладов XXXI студенческой научно-технической конференции 1980 / с. 52-55 https://www.ester.ee/record=b1319482*est

Генерирование операндов при синтезе тестов для микропроцессоров
Toomsalu, Arvo; **Ubar, Raimund-Johannes** Синтез и диагностика цифровых устройств и систем 1982 / с. 63-73 : илл https://www.ester.ee/record=b1328194*est https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b

Генерирование тестов для комбинационных схем с кратными неисправностями
Ubar, Raimund-Johannes Вопросы проектирования и расчета автоматических информационных систем : [Сборник статей] 1978 / с. 6-10

Генерирование тестов для микропроцессорных систем
Aasma, M.; **Kõlamets, A.** XXVII студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 19-21 апреля 1983 г : тезисы докладов. Часть 2 1983 / с. 14 https://www.ester.ee/record=b1571566*est

Генерирование тестов для цифровых схем при помощи модели альтернативных графов
Ubar, Raimund-Johannes Труды по электротехнике и автоматике : сборник статей. 14 1976 / с. 75-81 https://www.ester.ee/record=b2190768*est https://digikogu.taltech.ee/et/Item/aa35e320-87b1-405b-9cac-3b90c51867d1

Генерирование тестов микропроцессорных систем на модели АГ
Ubar, Raimund-Johannes Техническая диагностика : Тезисы докладов III Международного симпозиума ИМЕКО, Москва, окт. 1983 1983 / с. 100-103

Генерирование универсальных тестов для дискретных устройств на альтернативных графах
Ubar, Raimund-Johannes Методы синтеза и диагностирования цифровых схем 1985 / с. 51-60 : ил
https://www.ester.ee/record=b1302568*est https://digikogu.taltech.ee/et/Item/e00f2c15-fd8c-48ac-9963-76da1d62d592

Дедуктивной анализ тестов в синхронных цифровых схемах без обратных связей
Viilup, Agu; **Kitsnik, Peeter**; **Ubar, Raimund-Johannes** Материалы конференции "Автоматизация технического проектирования ЦВМ" (май-июнь 1977 г.) 1977 / с. 178-181

Декомпозиционный метод диагноза неисправностей в комбинационных схемах
Ubar, Raimund-Johannes Анализ и моделирование технических устройств и систем АСУТП 1978 / с. 3-22 : илл
https://www.ester.ee/record=b2191003*est https://digikogu.taltech.ee/et/Item/00fbff38-ccfb-411c-ad55-0c6b943b766b

Диагноз комбинационных схем при расширенном классе неисправностей
Ubar, Raimund-Johannes Материалы всесоюзной конференции "Автоматизированное техническое проектирование электронной аппаратуры", 5-6 июня 1979 г. 1979 / с. 177-180

Диагностика кратных неисправностей в комбинационных схемах
Viilup, Agu; **Ubar, Raimund-Johannes**; Heiter, U. Труды по электротехнике и автоматике : сборник статей. 11 1973 / с. 89-94 : илл https://www.ester.ee/record=b2190624*est https://digikogu.taltech.ee/et/Item/d6e57925-e104-44e1-a218-c5b3110d9996

Единый подход к решению задач тестового диагностирования дискретных систем
Ubar, Raimund-Johannes; **Lohuaru, Tõnu**; **Evartson, Teet** IX симпозиум по проблеме избыточности в информационных системах, 3-8 июня 1986 г. : тезисы докладов 1986 / с. 32-35

Единый подход к решению задач тестового диагностирования дискретных систем
Ubar, Raimund-Johannes; **Lohuaru, Tõnu**; **Evartson, Teet** IX симпозиум по проблеме избыточности в информационных системах, 3 июня - 8 июня 1986 года : Тезисы докладов 1986 / с. 32-35

Единый подход к синтезу тестов цифровых схем и систем
Ubar, Raimund-Johannes Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 75-81 : илл https://www.ester.ee/record=b1237891*est

Исследование и разработка методов анализа диагностических тестов для цифровых схем : автореферат ... кандидата технических наук (05.13.01)
Kitsnik, Peeter 1981 https://www.ester.ee/record=b1337813*est

Исследование и разработка методов анализа диагностических тестов для цифровых схем : диссертация на соискание ученой степени кандидата технических наук (05.13.01)
Kitsnik, Peeter 1980 https://www.ester.ee/record=b4632972*est

Исследование и разработка методов тестового диагностирования дискретных систем : автореферат ... доктора технических наук (05.13.13)
Ubar, Raimund-Johannes 1986 https://www.ester.ee/record=b1564280*est

Исследование и разработка методов управления поиском дефектов в цифровых схемах : автореферат .... кандидата технических наук (05.13.01)
Evartson, Teet 1986 https://www.ester.ee/record=b1301665*est

Комплекс средств диагностирования дискретных устройств
Ubar, Raimund-Johannes; Lohuaru, Tõnu Мир ПК 1991 / 1, с. 122-125 : ил

Локализация кратных неисправностей в цифровых схемах методом решения булевых дифференциальных уравнений
Ubar, Raimund-Johannes Системы и средства управления : межвузовский сборник научных трудов 1978 / с. 71-74
https://www.ester.ee/record=b2642693*est

Метод дедуктивного анализа тестов для логических схем
Viilup, Agu; **Kitsnik, Peeter**; **Ubar, Raimund-Johannes** Вопросы технической диагностики 1977 / с. [?]
https://www.ester.ee/record=b2353473*est

Метод диагноза неисправностей в последовательностных системах

Grigorjeva, Ksenja; **Ubar, Raimund-Johannes** Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 35-44 https://www.ester.ee/record=b1281890*est https://digikogu.taltech.ee/et/Item/8e0abfe2-9020-4ebd-85d1-fd67de0d1b30

Метод локализации неисправностей при проверке цифровых схем автоматическими тестерами
Viilup, Agu; **Lohuaru, Tõnu**; **Ubar, Raimund-Johannes** Анализ и моделирование технических устройств и систем АСУТП 1977 / с. 37-45 : илл https://www.ester.ee/record=b2190987*est https://digikogu.taltech.ee/et/Item/b7c66054-0b4f-4684-9453-442bc7e6e200

Метод сжатия диагностических словарей для логических схем
Suga, M.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с.135-136 https://www.ester.ee/record=b1306141*est

Метод эквивалентного преобразования диагностических словарей
Ubar, Raimund-Johannes Вопросы расчета и проектирования автоматических информационных систем 1975 / с. [?]

Методы тестового диагностирования дискретных систем
Ubar, Raimund-Johannes Машинное проектирование электронных устройств и систем 1986 / с. 57-69

Модель векторных альтернативных графов для описания цифровых систем
Ubar, Raimund-Johannes Вычислительная техника 1982 / с. 103-104

О выборе контролируемых параметров
Ubar, Raimund-Johannes Автоматика и вычислительная техника : АВТ : научно-теоретический журнал 1971 / с. 28-32 : илл https://www.ester.ee/record=b1908560*est

О генерировании тестов цифровых схем в реальном времени
Grigorjeva, Ksenja; **Ubar, Raimund-Johannes** XVII областная научно-техническая конференция по вопросам повышения эффективности и качества систем и средств управления (май 1981 года) : тезисы докладов 1981 / с. 112

О минимизации средного времени обнаружения неисправностей в технических устройствах
Ubar, Raimund-Johannes; Maslennikov, V.P. Вопросы управления процессами. Ч.1 1971 / с. 136-142

О моделировании длинных входных последовательностей в дискретных устройствах, содержащих счетные структуры
Ubar, Raimund-Johannes; **Evartson, Teet** Методы синтеза и диагностирования цифровых схем 1985 / с. 61-74 https://www.ester.ee/record=b1302568*est https://digikogu.taltech.ee/et/Item/e00f2c15-fd8c-48ac-9963-76da1d62d592

О проверке полноты контролирующих тестов цифровых схем
Ubar, Raimund-Johannes XV Областная научно-техническая конференция по системам и средствам управления, май 1979 года : Тезисы докладов Пермь / с. 74-75

О синтезе тестов для микропроцессорных БИС
Lohuaru, Tõnu; **Ubar, Raimund-Johannes** Проектирование и диагностика вычислительных средств 1987 / с. 30-42 : илл https://www.ester.ee/record=b1273275*est

О снижении комбинаторных трудностей при синтезе тестов для цифровых автоматов
Ubar, Raimund-Johannes Расчет и проектирование систем технической кибернетики 1983 / с. 111-119 : ил https://www.ester.ee/record=b1288991*est https://digikogu.taltech.ee/et/Item/7d7515af-76b7-4d35-89a7-e80367d5b635

О функциональном моделировании диагностических тестов в схемах ЦВМ
Vaher, V.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 133 https://www.ester.ee/record=b1306141*est

Об автоматическом синтезе тестов для цифровых объектов систем управления
Plakk, Mari; **Ubar, Raimund-Johannes** VII Всесоюзное совещание по проблемам управления, Минск, 21-25 ноября 1977. Кн. 3 1977 / с. 97-98

Об интерпретативном моделировании неисправностей в комбинационных логистических схемах
Viilup, Agu; **Kitsnik, Peeter**; **Ubar, Raimund-Johannes** Труды по электротехнике и автоматике : сборник статей. 11 1973 / с. 79-88 : илл https://www.ester.ee/record=b2190624*est https://digikogu.taltech.ee/et/Item/d6e57925-e104-44e1-a218-c5b3110d9996

Об общей постановке задач тестовой диагностики цифровых схем
Ubar, Raimund-Johannes Труды по электротехнике и автоматике : сборник статей. 14 1976 / с. 69-73 https://www.ester.ee/record=b2190768*est https://digikogu.taltech.ee/et/Item/aa35e320-87b1-405b-9cac-3b90c51867d1

Об одной задаче упорядочения множества элементов на временной ОСИ

Ubar, Raimund-Johannes Труды по электротехнике и автоматике : сборник статей. 8 1970 / с. 57-69 : илл https://www.ester.ee/record=b2189971*est https://digikogu.taltech.ee/et/Item/f65c4042-b55d-4b5b-b9b9-8a70cac2957d/

Обобщенная модель альтернативных графов для синтеза тестов цифровых систем
Ubar, Raimund-Johannes Расчет и проектирование систем технической кибернетики 1983 / с. 97-109 : ил https://www.ester.ee/record=b1288991*est https://digikogu.taltech.ee/et/Item/7d7515af-76b7-4d35-89a7-e80367d5b635

Обобщенный подход к многозначному моделированию цифровых схем на модели альтернативных графов
Voolaine, Andrus; Pall, Martin; **Ubar, Raimund-Johannes** Синтез и диагностика цифровых устройств и систем 1982 / с. 23-37 : илл https://www.ester.ee/record=b1328194*est https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b

Описание неисправностей цифровых устройств
Ubar, Raimund-Johannes Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 3-9 : илл https://www.ester.ee/record=b1264145*est https://digikogu.taltech.ee/et/Item/81bf2178-a9f8-417d-86c7-2000cca6a01e

Описание ЦВМ моделью векторных альтернативных графов с целью синтеза диагностических микропрограмм
Ubar, Raimund-Johannes Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 11-20 : илл https://www.ester.ee/record=b1264145*est https://digikogu.taltech.ee/et/Item/81bf2178-a9f8-417d-86c7-2000cca6a01e

Описание цифровых устройств моделью альтернативных графов
Ubar, Raimund-Johannes Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 11-33 : илл https://www.ester.ee/record=b1281890*est https://digikogu.taltech.ee/et/Item/8e0abfe2-9020-4ebd-85d1-fd67de0d1b30

Оптимизация процессов диагностирования цифровых устройств в реальном времени
Grigorjeva, Ksenja; **Lohuaru, Tõnu**; **Evartson, Teet**; **Ubar, Raimund-Johannes** Вычислительная техника : тезисы докладов республиканской конференции "Автоматизированное техническое проектирование электронной аппаратуры" (1–2 июня 1982 г.) 1982 / с. 144

Параллельное интерпретативное моделирование тестов для комбинационных логических схем
Puntso, T.; **Ubar, Raimund-Johannes** XX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР : тезисы докладов. Часть 1 1974 / с. 134 https://www.ester.ee/record=b1306141*est

Персональная среда проектирование цифровых систем
Raud, Rein; **Lohuaru, Tõnu**; **Ubar, Raimund-Johannes** Автоматизация проектирования электронной аппаратуры : Межвузовский тематический научный сборник 1989 / с. 39-43

Поиск неисправностей в цифровых схемах в режиме диалога
Ubar, Raimund-Johannes Вопросы технической диагностики : [межвузовский сборник] 1980 / с. 76-85 https://www.ester.ee/record=b4430898*est

Построение полных контролирующих тестов комбинационных схем
Ubar, Raimund-Johannes Eesti NSV Teaduste Akadeemia toimetised. Füüsika. Matemaatika = Известия Академии наук Эстонской ССР. Физика. Математика = Proceedings of Academy of Sciences of the Estonian SSR. Physics. Mathematics 1982 / lk. 418-427; ill. https://www.ester.ee/record=b1264310*est

Построение тестов для дискретных систем нам простых альтернативных графах
Voolaine, Andrus; Pall, M.; **Ubar, Raimund-Johannes** Тезисы докладов всесоюзной научно-технической конференции "Методы и средства борьбы с помехами в цифровой технике" 1986 / с. 88-89

Построение тестов для неисправностей комбинационных схем на основе анализа ортогональных дизъюнктивных нормальных форм, представляемых альтернативными графами
Matrosova, A.Yu.; Pleshkov, A.G.; **Ubar, Raimund-Johannes** Автоматика и телемеханика 2005 / с. 158-174 : ил http://mi.mathnet.ru/at1333

Построение тестов для проверки операционных частей дискретных систем
Ubar, Raimund-Johannes; **Lohuaru, Tõnu**; **Štraube, B.**; **Elst, G.** Машинное проектирование электронных устройств и систем 1988 / с. 65-77

Построение тестов цыфровых схем при помощи модели Алтернативных графов
Plakk, Mari; **Ubar, Raimund-Johannes** Автоматика и телемеханика 1980 / с. 152-163 : илл https://www.ester.ee/record=b1515055*est

Применение метода Монте-Карло для статистической оптимизации процессов контроля
Ubar, Raimund-Johannes; Maslennikov, V.P. Вопросы управления процессами. Ч.1 1971 / с. 129-135

Применение модели АГ для автоматизации синтеза тест-программ микропроцессорных БИС

Ubar, Raimund-Johannes Электронная техника. Серия 8, Управление качеством, стандардизация, метрология, испытания : научно-технический сборник 1985 / с. 110-113 https://www.ester.ee/record=b2160764*est

Применение модели альтернативных графов при синтезе тестов для комбинационных схем
Plakk, Mari; **Ubar, Raimund-Johannes** Анализ и моделирование технических устройств и систем АСУТП 1977 / с. 3-13 : илл https://www.ester.ee/record=b2190987*est https://digikogu.taltech.ee/et/Item/b7c66054-0b4f-4684-9453-442bc7e6e200

Проектирование автоматизированных систем контроля бортового оборудования летательных аппаратов
Seleznjov, A.; Dobritsa, B.; Ubar, Raimund-Johannes 1983

Проектирование диагностических тестов для микропроцессорных БИС и систем
Einasto, N.; **Ubar, Raimund-Johannes** XXX студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 8-10 апреля 1986 года : тезисы докладов. Том II, Автоматика. Энергетика. Механика. Химия 1986 / с. 40 https://www.ester.ee/record=b1305565*est

Проектирование контролепригодных дискретных систем : учебное пособие
Ubar, Raimund-Johannes 1988 https://www.ester.ee/record=b1225400*est

Профессиональная среда проектирования цифровых систем
Raud, R.; **Lohuaru, Tõnu**; **Ubar, Raimund-Johannes** Автоматизация проектирования электронной аппаратуры : межвузовский тематический научный сборник 1989 / с. 39-43

Раймунд Убар: ученые делают свое дело, политики - свое : [интервью с Р. Убаром]
Ubar, Raimund-Johannes Босс : бизнес, организаця, стратегия, системы 2012 / с. 57-58 : ил

Расчет и проектирование систем технической кибернетики
1984 https://www.ester.ee/record=b1549179*est https://digikogu.taltech.ee/et/Item/99cc4681-4aa3-466a-b6da-b76f575d0f1e

Решение задач диагностики цифровых устройств модели альтернативных графов
Kurilova, L.; **Popova, S.**; **Tulina, M.**; **Ubar, Raimund-Johannes**; **Jakubovitš, M.** XXV студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 21-23 апреля 1981 года : тезисы докладов. Том 2, Автоматика. Энергетика. Механика. Химия 1981 / с. 39 https://www.ester.ee/record=b1322629*est

Решение задач проектирования тестов микроэлектронных устройств при помощи АГ
Ubar, Raimund-Johannes Тезисы докл. всесоюзн. школы-семинара "Диагностика, надежность контроль" 1990 / с. 65

Синтез парных тестов комбинационных схем
Plakk, Mari; **Ubar, Raimund-Johannes** Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 45-68 : илл https://www.ester.ee/record=b1281890*est https://digikogu.taltech.ee/et/Item/8e0abfe2-9020-4ebd-85d1-fd67de0d1b30

Синтез тестов для цифровых схем
Plakk, Mari; **Ubar, Raimund-Johannes** XIV областная научно-техническая конференция по системам и средствам управления (май 1978 г.) : тезисы докладов 1978 / с. 78-79

Система автоматического тест-программ для вычислительных устройств
Alango, Villem; **Kont, Toomas**; **Ubar, Raimund-Johannes** I международная научно-техническая конференция САПР СВТ 89 : доклады. Ленинград, 17-21 апреля 1989 г. Секция 2. Автоматизация логического проектирования СВТ. 1989 / с. 23-31

Система генерирования тестов для микропроцессоров
Ubar, Raimund-Johannes; **Dušina, Julia**; **Zaugarov, Viktor**; Крупнова Е.; **Storožev, Sergei** Proceedings of international conference "Technical Diagnostics-93", St.-Peterburg, June 8-10, 1993 1993 / p. 87-89

Тестовая диагностика цифровых устройств : учебное пособие. II, Синтез и анализ тестов. Дешифрация диагностических экспериментов
Ubar, Raimund-Johannes 1981 https://www.ester.ee/record=b1326795*est

Тестовое диагностирование дискретных систем на модели АГ
Ubar, Raimund-Johannes Техническая диагностика : VI всесоюзное совещание, Ростов н/Д, май 1987 г. : Тезисы докладов 1987 / с. 155

Универсальный подход к автоматизации проектирования тестов для широкого класса дискретных объектов
Ubar, Raimund-Johannes Машинное проектирование электронных устройств и систем 1986 / с. 70-92

Управление процессами диагноза логических схем
Toome, T.; **Ubar, Raimund-Johannes**; **Evartson, Teet** Тезисы докладов XXXI студенческой научно-технической конференции

1980 / с. 55-57 https://www.ester.ee/record=b1319482*est

Управление процессом пойска дефектов в цифровых схемах содержащих счётные структуры
Viilup, Agu; **Ubar, Raimund-Johannes**; **Evartson, Teet** Межреспубликанская школа-семинар по технической диагностике, 8-12 октября 1984 года : тезисы докладов 1984 / с. 28-32 https://www.ester.ee/record=b1237891*est

Формальный синтез тестов для микропроцессоров
Toomsalu, Arvo; **Ubar, Raimund-Johannes** XVII областная научно-техническая конференция по вопросам повышения эффективности и качества систем и средств управления (май 1981 г.): Тезисы докладов 1981 / с. 111-112

Формирование тест-программ для микропроцессорных БИС при автоматическом генерировании тестов
Alango, Villem; **Kont, Toomas**; **Ubar, Raimund-Johannes** Машинное проектирование электронных устройств и систем 1988 / с. 78-87

Формулы для дедуктивного анализа тестов в синхронных последовательностных схемах
Kitsnik, Peeter; **Ubar, Raimund-Johannes** Анализ и моделирование технических устройств и систем АСУТП 1977 / с. 15-23 : илл https://www.ester.ee/record=b2190987*est https://digikogu.taltech.ee/et/Item/b7c66054-0b4f-4684-9453-442bc7e6e200

Электротехника и автоматика
Rüstern, Ennu; **Leis, Paul**; **Sudnitsõn, Aleksander**; **Viies, Vladimir**; **Berkman, Boriss**; **Keevallik, Andres**; **Kruus, Margus**; **Ubar, Raimund-Johannes**; **Alango, Villem**; **Kont, Toomas**; **Grigorjeva, Ksenja**; Einasto, N.; **Evartson, Teet**; **Gerasimtšuk, Valeri**; Mahhitko, V.P.; Šendrik, M.G.; **Tamm, Boris, inform.** 1986 https://www.ester.ee/record=b1296477*est

Электротехника и автоматика
Rüstern, Ennu; **Keevallik, Andres**; **Kruus, Margus**; **Salum, Kaja**; **Berkman, Boriss**; **Tammemäe, Kalle**; **Alango, Villem**; **Kont, Toomas**; **Ubar, Raimund-Johannes**; Lohuaru, Tõnu; Štraube, B.; Elst, G.; Bombik, B.; **Viies, Vladimir**; Gallai, S.; **Rang, Toomas**; **Laansoo, Ants**; **Männama, Vello**; **Pikkov, Otto**; **Gurjanov, Boris**; **Opotski, Aleksei**; **Velmre, Enn** 1988
https://www.ester.ee/record=b1256708*est

Электротехника и автоматика
Mägi, Harri; **Velmre, Enn**; **Pikkov, Mihhail**; Orro, S.; **Rang, Toomas**; **Gurjanov, Boris**; **Kruus, Margus**; **Salum, Kaja**; **Berkman, Boriss**; **Keevallik, Andres**; **Kasirova, Lilia**; **Kruus, Margus**; **Ellervee, Peeter**; **Ubar, Raimund-Johannes**; **Grigorjeva, Ksenja**; **Kont, Toomas** 1989 https://www.ester.ee/record=b1285446*est