A five step refactoring process : improving software design properly
Põld, Janari; **Kalja, Ahto**; **Robal, Tarmo** Databases and information systems : proceedings of the Eighth International Baltic Conference, Baltic DBAMPIS 2008 : Tallinn, June 2-5, 2008 2008 / p. 37-48 : ill

Address-based data processing over N-ary trees
Sklyarov, Valery; Skliarova, Iouliia; **Kruus, Margus**; **Mihhailov, Dmitri**; **Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

American sign language character recognition using convolutional neural networks
Abdullah, Atesam; Ali, Nisar; Ali, Raja Hashim; **Abideen, Zain Ul**; Ijaz, Ali Zeeshan; Bais, Abdul 2023 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE) : Regina, SK, Canada, 24-27 September 2023 2023 / p. 165-169
https://doi.org/10.1109/CCECE58730.2023.10288799

An OLAP cube based development method of information systems
Lemmik, Rivo Proceedings of the 7th International Conference of DAAAM Baltic Industrial Engineering : 22-24th April 2010, Tallinn, Estonia. [II] 2010 / p. 584-588

Application of extensible processing platforms for experiments with FPGA-based circuits
Sklyarov, Valery; Skliarova, Iouliia; Silva, João; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 467-471 : ill

Architectural exploration tasks for on-chip embedded systems
Reinsalu, Uljana; **Arhipov, Anton**; **Ellervee, Peeter** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 171-174 : ill

Architecture of a list-based virtual machine for implementing COBOL : a thesis submitted to Tallinn Technical University in partial fulfilment of the requirements for the degree of master of engineering : magistritöö
Taveter, Kuldar 1995 http://www.ester.ee/record=b1756467*est

Assessment of diagnostic test for automated bug localization
Tihhomirov, Valentin; **Tšepurov, Anton**; **Jenihhin, Maksim**; **Raik, Jaan**; **Ubar, Raimund-Johannes** LATW2013 : 14th IEEE Latin-American Test Workshop, Cordoba, Argentina, April 3-5, 2013 : [proceedings] 2013 / [6] p. : ill

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele
Gorev, Maksim 2015 https://digi.lib.ttu.ee/i/?3953

At-speed testing of inter-die connections of 3D-SICs in the presence of shore logic
Shibin, Konstantin; Chickermane, Vivek; Keller, Brion; Papameletis, Christos; Marinissen, Erik Jan 2015 Asian Test Symposium : ATS 2015 : 22-25 November 2015, Mumbai, Maharashtra, India : proceedings 2015 / p. 79-84 : ill http://dx.doi.org/10.1109/ATS.2015.21

Automated design error debug using high-level decision diagrams and mutation operators
Raik, Jaan; **Repinski, Urmas**; **Tšepurov, Anton**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; **Jenihhin, Maksim** Microprocessors and microsystems 2013 / p. 505-513 : ill

Automated design error localization in RTL designs
Jenihhin, Maksim; **Tšepurov, Anton**; **Tihhomirov, Valentin**; **Raik, Jaan**; **Hantson, Hanno**; **Ubar, Raimund-Johannes**; Bartsch, Günter; Meza Escobar, Jorge Hernan; Wuttke, Heinz-Dietrich IEEE design & test of computers 2014 / p. 83-92 : ill
http://dx.doi.org/10.1109/MDAT.2013.2271420

Automatic diagnosis of simple design errors
Ubar, Raimund-Johannes; Borrione, Dominique TIMA annual report 1998 1999 / p. 97-98

Automatic diagnosis of simple design errors
Ubar, Raimund-Johannes; Borrione, Dominique Techniques of Informatics and Microelectronics for Computer Architecture 1999 / p. 91

Challenges for future system-on-chip design
Hollstein, Thomas; Peng, Zebo; **Ubar, Raimund-Johannes**; Glesner, Manfred Circuit Paradigm in the 21st Century : ECCTD '01 : proceedings of the 15th European Conference on Circuit Theory and Design : Helsinki University of Technology, Finland, 28th-31st August 2001. Vol 3 2001 / p. 173-176

Code compaction within CGRAs
Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** Proceedings of the 8th Annual Conference of

the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 133-136 : ill

Customizable compression architecture for efficient configuration in CGRAs
Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines : FCCM 2014 : 11-13 May 2014, Boston, Massachusetts, USA : proceedings 2014 / p. 31 : ill

Customization methodology of a Coarse Grained Reconfigurable Architecture
Azad, Siavoosh Payandeh; Farahini, Nasim; Hemani, Ahmed Norchip : 32nd NORCHIP Conference, 27-28 October 2014, Tampere, Finland 2014 / [4] p. : ill

Deadlock-free generic routing algorithms for 3-dimensional Networks-on-Chip with reduced vertical link density topologies
Ying, Haoyuan; Jaiswal, Ashok; **Hollstein, Thomas**; Hofmann, Klaus Journal of systems architecture 2013 / p. 528-542 : ill

Design space exploration in multi-level computing systems
Sklyarov, Valery; Skliarova, Iouliia; Silva, João; **Sudnitsõn, Aleksander** CompSysTech'14 : 15th International Conference on Computer Systems and Technologies : Ruse, Bulgaria, June 27-28, 2014 2014 / p. 40-47 : ill

Digitaalseadmete struktuuri projekteerimine : õppevahend
Ariste, Andri 1978 https://www.ester.ee/record=b1305228*est

An efficient FPGA-based architecture for contractive autoencoders
Kerner, Madis; **Tammemäe, Kalle**; **Raik, Jaan**; Hollstein, Thomas 2020 IEEE 28th Annual International Symposium on Field-Programmable Custom Computing Machines (FCCM), 3 – 6 May 2020, Fayetteville, Arkansas : proceedings 2020 / p. 230−230 https://doi.org/10.1109/FCCM48280.2020.00062.

Execution of dataflow process networks on OpenCL platforms
Lund, Wictor; Kanur, Sudeep; Ersfolk, Johan; **Tsiopoulos, Leonidas** 23rd Euromicro International Conference on Parallel, Distributed, and Network-Based Processing : PDP 2015 : 4-6 March 2015, Turku, Finland : proceedings 2015 / p. 618-625 : ill https://doi.org/10.1109/PDP.2015.29

Exploring deep learning based object detection architectur
Saddique, Muhammad Saddique; Raza, Ahsan; **Abideen, Zain Ul**; Khan, Shah Nawaz 2020 17th International Bhurban Conference on Applied Sciences and Technology (IBCAST), Islamabad, Pakistan, 2020 2020 / p. 255-259 https://doi.org.10.1109/IBCAST47879.2020.9044558

Extensible open-source framework for translating RTL VHDL IP cores to SystemC
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** Proceedings of the 2013 IEEE 16th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 8-10, 2013, Karlovy Vary, Czech Republic 2013 / p. 112-115

Fast and optimized task allocation method for low vertical link density 3-Dimensional Networks-on-Chip based many core systems
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus Proceedings : Design, Automation & Test in Europe : Grenoble, France, March 18-22, 2013 2013 / p. 1777-1782 : ill

Fast iterative circuits and RAM-based mergers to accelerate data sort in software/hardware systems
Sklyarov, Valery; Skliarova, Iouliia; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** Proceedings of the Estonian Academy of Sciences 2017 / p. 323-335 : ill https://doi.org/10.3176/proc.2017.3.07 http://www.ester.ee/record=b2355998*est

FPGA-based accelerators for parallel data sort
Sklyarov, Valery; Skliarova, Iouliia; **Sudnitsõn, Aleksander** Applied computer systems 2014 / p. 53-63 : ill

Functional self-test of high-performance pipe-lined signal processing architectures
Gorev, Maksim; **Ubar, Raimund-Johannes**; **Ellervee, Peeter**; **Devadze, Sergei**; **Raik, Jaan**; **Min, Mart** Microprocessors and microsystems 2015 / p. 909-918 : ill http://dx.doi.org/10.1016/j.micpro.2014.11.002

GSNoC — the comprehensive design platform for 3-dimensional Networks-on-Chip based many core embedded systems
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus Proceedings of the 2013 International Conference on High Performance Computing & Simulation (HPCS 2013) : July 1-July 5, 2013, Helsinki, Finland 2013 / p. 217-223 : ill

Hardware trojan insertion in finalized layouts : from methodology to a silicon demonstration
Perez, Tiago Diadami; **Pagliarini, Samuel Nascimento** IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2023 / p. 2094-2107 https://doi.org/10.1109/TCAD.2022.3223846 Journal metrics at Scopus Article at Scopus Journal metrics at WOS Article at WOS

Hardware/software co-design in extensible processing platforms for combinatorial search algorithms
Skliarova, Iouliia; Sklyarov, Valery; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 462-466 : ill

A hardware/software co-design reconfigurable network-on-chip FPGA emulation method
Ying, Haoyuan; **Hollstein, Thomas**; Hofmann, Klaus 2014 9th International Symposium on Reconfigurable and Communication-Centric Systems-on-Chip (ReCoSoC) : Montpellier, France, 26-28 May, 2014 2014 / [8] p. : ill

High-level implementation-independent software-based self-test for RISC type microprocessors = Mikroprotsessorite tarkvarapõhine implementatsioonist mittesõltuv funktsionaalne enesekontroll
Oyeniran, Adeboye Stephen 2020 https://digikogu.taltech.ee/et/Item/08a75fbb-3f71-4fe4-b3d0-3f37a9a5f36d

Hybrid BIST energy minimisation technique for system-on-chip testing
Jervan, Gert; **Peng, Zebo**; **Shchenova, Tatjana**; Ubar, Raimund-Johannes IEE proceedings computers & digital techniques 2006 / 4, p. 208-216 : ill https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=5ae755d323ccba87f8ff886334e3dd6d33560874

Hybrid BIST scheduling for NoC-based SoCs
Jervan, Gert; **Shchenova, Tatjana**; **Ubar, Raimund-Johannes** Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 141-144 : ill https://ieeexplore.ieee.org/document/4126966

Implementation of parallel operations over streams in extensible processing platforms
Sklyarov, Valery; Skliarova, Iouliia; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) : August 4-7, 2013, Columbus, Ohio : [proceedings] 2013 / p. 852-855 : ill

Infotehnoloogia. Sõnastik. Osa 11, Töötlusseadmed
Hanson, Vello; **Agur, Ustus**; **Kalja, Ahto**; **Võhandu, Leo** 1999 https://www.ester.ee/record=b1211017*est

Jini tehnoloogiast
Küngas, Peep Arvutimaailm 2000 / 8, lk. 45 https://artiklid.elnet.ee/record=b1004987*est

Jäljevahemälu
Toomsalu, Arvo A & A 2002 / 2, lk. 8-19 : ill https://artiklid.elnet.ee/record=b1009485*est

Latest trends in hardware security and privacy
Di Natale, Giorgio; Regazzoni, Francesco; Albanese, Vincent; Lhermet, Frank; Loisel, Yann; Sensaoui, Abderrahmane; **Pagliarini, Samuel Nascimento** 33rd IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : ESA-ESRIN, Italy (On-line Virtual Event),October 19–21, 2020 2020 / 4 p. : ill https://doi.org/10.1109/DFT50435.2020.9250816

Logic IP for low-cost IC design in advanced CMOS nodes
Isgenc, Mehmet Meric; Martins, Mayler G.A.; Zackriya, V. Mohammed; **Pagliarini, Samuel Nascimento**; Pileggi, Larry IEEE Transactions on Very Large Scale Integration (VLSI) Systems 2020 / p. 585-595 https://doi.org//10.1109/TVLSI.2019.2942825

MASI-arhitektuuriga võrguprotsessor
Toomsalu, Arvo A & A 2004 / 3, lk. 7-18

Memristive device based circuits for computation-in-memory architectures
Lebdeh, Muath Abu; **Reinsalu, Uljana**; Nguyen, Hoang Anh Du; Wong, Stephan; Hamdioui, Said 2019 IEEE International Symposium on Circuits and Systems (ISCAS) : proceedings 2019 / 5 p. : ill https://doi.org/10.1109/ISCAS.2019.8702542 Conference proceedings at Scopus Article at Scopus Article at WOS

Mikroprotsessorsüsteemid : kursuseprojekti juhendmaterjal
Toomsalu, Arvo 1998 https://www.ester.ee/record=b1061287*est

Model Driven Architecture
Leis, Paul A & A 2004 / 1, lk. 13-20 : ill https://artiklid.elnet.ee/record=b1014997*est

Monomikroprotsessorite arhitektuuri põhilisi arengusuundi
Toomsalu, Arvo A & A 2005 / 3, lk. 15-23 ; 4, lk. 13-29 : ill

Morphable compression architecture for efficient configuration in CGRAs
Jafri, Syed Mohammad Asad Hassan; Tajammul, Muhammad Adeel; **Ellervee, Peeter** 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 42-49 : ill

Multi- ja andmeskalaarse arhitektuuriga protsessorid
Toomsalu, Arvo A & A 2005 / 6, lk. 15-27

Mõtisklusi agiilarhitektuurist
Leis, Paul A & A 2011 / lk. 22-27 : ill https://artiklid.elnet.ee/record=b2472199*est

Novel architectures for contractive autoencoders with embedded learning
Kerner, Madis; **Tammemäe, Kalle**; **Raik, Jaan**; **Hollstein, Thomas** 2020 17th Biennial Baltic electronics conference, Tallinn, Estonia, October 6-8, 2020 : proceedings 2020 / 6 p. : ill https://doi.org/10.1109/BEC49624.2020.9277246

On proving the concept of an ontology aided software refactoring tool
Põld, Janari; **Robal, Tarmo**; **Kalja, Ahto** Databases and information systems : tenth international Baltic conference on databases and information systems : local proceedings, materials of doctoral consortium : Vilnius, Lithuania, July 8-11, 2012 2012 / p. 179
https://www.researchgate.net/publication/287294774_On_proving_the_concept_of_an_ontology_aided_software_refactoring_tool

Operatsioonautomaadid digitaalarvutites : metoodiline materjal
1987 https://www.ester.ee/record=b1234461*est

Optimization methodologies for Cycle-Accurate SystemC models converted from RTL VHDL
Saif Abrar, Syed; **Jenihhin, Maksim**; **Raik, Jaan** IP-SoC 2013 : IP embbeded system conference and exhibition : Grenoble, France, November 6-7, 2013 2013

Parallel pseudo-exhaustive testing of array multipliers with data-controlled segmentation
Oyeniran, Adeboye Stephen; **Azad, Siavoosh Payandeh**; **Ubar, Raimund-Johannes** 2018 IEEE International Symposium on Circuits and Systems (ISCAS) : 27-30 May 2018, Florence, Italy : proceedings 2018 / 5 p.: ill
https://doi.org/10.1109/ISCAS.2018.8350936 Conference proceedings at Scopus Article at Scopus Article at WOS

Personaalarvutid mikroprotsessoril 80486. Sise- ja välisseadmete liidesed, matemaatikaprotsessorid, jõudlustestid
Toomsalu, Arvo 1992 https://www.ester.ee/record=b1064225*est

Perspektiivid voogtöötluses
Aarna, Agu, 1983- A & A 2008 / lk. 29-36 : ill https://artiklid.elnet.ee/record=b1021440*est

Polymorphic configuration architecture for CGRAs
Jafri, Syed Mohammad Asad Hassan; **Tajammul, Muhammad Adeel**; Hermani, Ahmed; Paul, Kolin; Plosila, Juha; **Ellervee, Peeter**; Tenhunen, Hannu IEEE transactions on Very Large Scale Integration (VLSI) Systems 2016 / p. 403-407 : ill
http://dx.doi.org/10.1109/TVLSI.2015.2402392

Post-RISC-arhitektuur
Toomsalu, Arvo A & A 2001 / 2, lk. 8-14 ; 3, lk. 7-16 https://artiklid.elnet.ee/record=b1006602*est

Preventing distillation-based attacks on Neural Network IP
Grailoo, Mahdieh; **Abideen, Zain Ul**; **Leier, Mairo**; **Pagliarini, Samuel Nascimento** arXiv.org 2022 / 7 p. : ill
https://doi.org/10.48550/arXiv.2204.00292

Processing N-ary trees in reconfigurable hardware
Sklyarov, Valery; **Skliarova, Iouliia**; **Sudnitsõn, Aleksander** 2013 25th International Conference on Microelectronics (ICM) : 15–18 December 2013, Beirut-Lebanon 2013 / p. 13-16 : ill

Protsessor mälus
Toomsalu, Arvo A & A 2001 / 4, lk. 9-16 https://artiklid.elnet.ee/record=b1007646*est

Que vadis, mikrokontroller?
Toomsalu, Arvo A & A 2010 / 1, lk. 9-16 https://artiklid.elnet.ee/record=b1965433*est

Rejuvenation of NBTI-impacted processors using evolutionary generation of assembler programs
Pellerey, Francesco; **Jenihhin, Maksim**; Squillero, Giovanni; **Raik, Jaan**; Sonza Reorda, Matteo; **Tihhomirov, Valentin**; **Ubar, Raimund-Johannes** 2016 IEEE 25th Asian Test Symposium : 21-24 November 2016, Hiroshima, Japan 2016 / p. 304-309 : ill
https://doi.org/10.1109/ATS.2016.57

RISC-mikroprotsessorite arhitektuur
Toomsalu, Arvo 1995 https://www.ester.ee/record=b1069536*est

Runtime contention and bandwidth-aware adaptive routing selection strategies for networks-on-chip
Samman, Faizal; **Hollstein, Thomas**; Glesner, Manfred IEEE transactions on parallel and distributed systems 2013 / p. 1411-1421 : ill

Scene parsing using Fully Convolutional Network for Semantic Segmentation

Ali, Nisar; Ijaz, Ali Zeeshan; Ali, Raja Hashim; **Abideen, Zain Ul**; Bais, Abdul 2023 IEEE Canadian Conference on Electrical and Computer Engineering (CCECE), Regina, SK, Canada, 2023 2023 / p. 180-185 https://doi.org.10.1109/CCECE58730.2023.10288934

See mitmetahuline rööpsus
Tammemäe, Kalle A & A 2006 / 2, lk. 7-12 : ill https://artiklid.elnet.ee/record=b1019098*est

Self-aware architecture to support partial control of emergent behavior
Mõtus, Leo; **Meriste, Merik**; **Preden, Jürgo-Sören**; **Pahtma, Raido** 2012 7th International Conference on System of Systems Engineering : July 16-19, 2012, Genova, Italy : proceedings 2012 / p. 422-427 : ill https://ieeexplore.ieee.org/document/6384148

Self-organization in ad hoc wireless networks
Kirt, Toomas; **Anier, Aivo** BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 149-152 : ill

SHARC-arhitektuuriga signaaliprotsessorite rakendamine infohankesüsteemides
Müürsepp, Ivo A & A 2005 / 4, lk. 38-45 : ill

Software architecture for modern telehealth care systems
Kuusik, Alar; **Reilent, Enar**; Lõõbas, Ivor; **Parve, Marko** Advances on information sciences and service sciences 2011 / p. 141-151

Software architecture for swarm mobile robots
Vain, Jüri; **Tammet, Tanel**; **Kuusik, Alar**; **Reilent, Enar** BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 231-234 : ill

Solving computationally intensive problems in reconfigurable hardware : a case study
Skliarova, Iouliia; Vallejo, Tiago; Sklyarov, Valery; **Sudnitsõn, Aleksander**; **Kruus, Margus** Journal of convergence information technology (JCIT) : an international journal 2013 / p. 601-609 : ill

SPARC-V8- ja V9-arhitektuuriga mikroprotsessorid
Toomsalu, Arvo Arvutustehnika ja Andmetöötlus 1995 / 7, lk. 14-23: ill

Stateful runners of effectful computations
Uustalu, Tarmo Electronic notes in theoretical computer science 2015 / p. 403-421 http://dx.doi.org/10.1016/j.entcs.2015.12.024

SuperH-arhitektuuriga protsessortuum kiipsüsteemidele
Toomsalu, Arvo A & A 2001 / 1, lk. 11-18 : ill https://artiklid.elnet.ee/record=b1006239*est

Sülemiintellektitehnika
Leis, Paul A & A 2007 / 1, lk. 3-5 : ill https://artiklid.elnet.ee/record=b1020322*est

zamiaCAD : shall we dance?
Jenihhin, Maksim Open Source Tools for Verification : DVClub 14 January 2013 2013 / 1 p

zamiaCAD : understand, develop and debug hardware designs
Jenihhin, Maksim; **Tihhomirov, Valentin**; **Saif Abrar, Syed**; **Raik, Jaan**; Bartsch, Günter DUHDe : 1st Workshop on Design Automation for Understanding Hardware Designs : March 28, 2014 : Friday Workshop at DATE 2014, Dresden, Germany 2014 / p. 1-6

Zynq-based system for extracting sorted subsets from large data sets
Sklyarov, Valery; Skliarova, Iouliia; **Rjabov, Artjom**; **Sudnitsõn, Aleksander** Journal of microelectronics, electronic components and materials 2015 / p. 142-152 : ill

Theses of Tallinn University of Technology. C, Thesis on informatics and system engineering = [Tallinna Tehnikaülikooli väitekirjad]. C, Informaatika ja süsteemitehnika, 1406-4731 ; 80
Reilent, Enar 2012

A 3-D crossbar architecture for both pipeline and parallel computations
Aljafar, Muayad J.; Acken, John M. IEEE Transactions on Circuits and Systems I : regular papers 2021 / p. 4456-4469 https://doi.org/10.1109/TCSI.2021.3108564 https://pdxscholar.library.pdx.edu/cgi/viewcontent.cgi?article=1680&context=ece_fac

TransMem : a memory architecture to support dynamic remapping and parallelism in low power high performance CGRAs
Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Hemani, Ahmed; **Ellervee, Peeter** 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation : PATMOS 2016 : September, 21st to 23th 2016, Bremen,

Germany : proceedings 2016 / p. 92-99 : ill https://doi.org/10.1109/PATMOS.2016.7833431

Ultra-low latency NoC testing via pseudo-random test pattern compaction
Tatenguem, Herve; **Govind, Vineeth**; **Raik, Jaan** SoC 2012 : International Symposium on System-on-Chip 2012 : Tampere, Finland, October 11-12, 2012 2012 / 6 p. : ill https://ieeexplore.ieee.org/document/6376370

VHDL design debug framework based on zamiaCAD
Tihhomirov, Valentin; **Tšepurov, Anton**; **Saif Abrar, Syed**; **Jenihhin, Maksim**; **Raik, Jaan** DATE 2013 : Design Automation and Test in Europe, March 18-22, 2013, Grenoble, France 2013 / [1] p. : ill