

Assembling low-level tests to high-level symbolic test frames

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings [of the] 15th NORCHIP Conference, Tallinn, 10-11 November 1997 1997 / p. 275-280: ill

Automatic test generation system for VLSI

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the First Electronic Circuits and Systems Conference : Bratislava, Slovakia, September 4-5, 1997 1997 / p. 255-258

CAD software for digital test and diagnostics

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of International Conference on Design and Diagnostics of Electronic Circuits and Systems, Ostrava, Czech Republik, May 12-14, 1997 1997 / p. 35-40

DECIDER : a decision diagram based hierarchical test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 2nd International Workshop on Design and Diagnostics of Electronic Circuits and Systems, Szczyrk, Poland, September 2-4, 1998 1998 / p. 269-273
<https://www.ida.liu.se/labs/eslab/publications/pap/db/DDECS98.pdf>

A decision diagram based hierarchical test pattern generator

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 159-162: ill

Fast and efficient static compaction of test sequences using bipartite graph representations

Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes ECS'99 : proceedings of the 2nd Electronic Circuits and Systems Conference : September 6-8, 1999, Bratislava, Slovakia 1999 / p. 17-20

Fault model and test synthesis for RISC-processors

Ubar, Raimund-Johannes; Markus, Antti; Jervan, Gert; Raik, Jaan BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 229-232: ill

A hierarchical automatic test pattern generator based on using alternative graphs

Brik, Marina; Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 4th International Workshop Mixed Design of Integrated Circuits and Systems : MIXDES'97 : Poznan, Poland, 12-14 June 1997 1997 / p. 415-420

Hierarchical test generation for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Mixed design of integrated circuits and systems 1998 / p. 131-136: ill https://link.springer.com/chapter/10.1007/978-1-4615-5651-0_20

Hierarchical test generation with multi-level decision diagram models

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 7th IEEE North Atlantic Test Workshop, West Greenwich RI, USA, May 28-29, 1998 1998 / p. 26-33
https://www.academia.edu/67811738/Hierarchical_Test_Generation_with_Multi_Level_Decision_Diagram_Models?hb-g-sw=7883185

Low-cost CAD system for teaching digital test

Ubar, Raimund-Johannes; Raik, Jaan; Paomets, Priidu; Ivask, Eero; Jervan, Gert; Markus, Antti Microelectronics education : proceedings of the European Workshop, Grenoble, France, 5-6 Feb 1996 1996 / p. 185-188

Mixed-level deterministic-random test generation for digital systems

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 335-340

Mixed-level test generator for digital systems

Brik, Marina; Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 1997 / 4, p. 271-282 : ill

A set of tools for estimating quality of built-in self-test in digital circuits

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the International Symposium on Signals, Circuits and Systems, Iasi (Romania), October 2-3, 1997 1997 / p. 362-365

Teaching test and design for testability with TURBO-TESTER software

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 3rd Workshop on Mixed Design of Integrated Circuits and Systems, Lodz, May 1996 1996 / p. 589-594

Test set minimization using bipartite graphs

Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes BEC'98 : the 6th Biennial Conference on Electronics and Microsystems Technology, October 7-9, 1998, Tallinn, Estonia : proceedings 1998 / p. 175-178: ill

Turbo tester : a CAD system for teaching digital test

Jervan, Gert; Markus, Antti; Paomets, Priidu; Raik, Jaan; Ubar, Raimund-Johannes Microelectronics education : proceedings of the 2nd European Workshop held in Noordwijkerhout, The Netherlands, 14-15 May 1998 1998 / p. 287-290: ill
https://link.springer.com/chapter/10.1007/978-94-011-5110-8_66

VHDL based test generation system

Jervan, Gert; Markus, Antti; Raik, Jaan; Ubar, Raimund-Johannes Proceedings of the 5th Electronic Devices and Systems Conference, Brno, June 11-12, 1998 1998 / p. 145-148