

Acceleration of recursive data sorting over tree-based structures

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Elektronika ir elektrotehnika = Electronics and electrical engineering 2011 / p. 51-56 : ill <https://eejournal.ktu.lt/index.php/elt/article/view/612>

Address-based data processing over N-ary trees

Sklyarov, Valery; Skliarova, Iuliia; **Kruus, Margus; Mihhailov, Dmitri; Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

Advanced topics of FSM design using FPGA educational boards and web-based tools

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 446-449 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5742086>

An approach to synthesis of mixed synchronous/asynchronous digital devices

Sudnitsõn, Aleksander 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings 2002 / p. 695-698

Analysis and comparison of attainable hardware acceleration in all programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Sudnitsõn, Aleksander** Euromicro Conference on Digital System Design : DSD 2015 : 26-28 August 2015, Funchal, Madeira, Portugal : proceedings 2015 / p. 345-352 : ill <http://dx.doi.org/10.1109/DSD.2015.45>

Application of extensible processing platforms for experiments with FPGA-based circuits

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Rjabov, Artjom; Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 467-471 : ill
<https://doi.org/10.1109/MELCON.2014.6820579> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Application-specific hardware accelerator for implementing recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Proceedings of the IEEE International Conference on Field Programmable Technology (FPT'10) : Beijing, China Dec. 8-10, 2010 2010 / p. 269-272 : ill
<https://ieeexplore.ieee.org/document/5681486>

Asynchronous e-learning resources for hardware design issues

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Proceedings of the International Conference on Computer Systems and Technologies (e-learning) : CompSysTech'04 : Rousse, Bulgaria, 17-18 June 2004 / p. IV.11-1 - IV.11-6 : ill https://www.researchgate.net/publication/234797327_Asynchronous_e-learning_resources_for_hardware_design_issues

A CAD system for decomposition oriented synthesis

Keevallik, Andres; Sudnitsõn, Aleksander; Udre, Jüri Proceedings of the International Conference "Computer-Aided Design of Discrete Devices", Minsk, 1995 1995 / p. 153-154

Computational kernel extraction for synthesis of power-managed sequential components

Sudnitsõn, Aleksander Proceedings of the 9th IEEE International Conference on Electronics, Circuits and Systems : ICECS'2002, Dubrovnik, Croatia 2002 / p. 749-752 <https://ieeexplore.ieee.org/abstract/document/1046277>

Computer aided design support of FSM multiplicative decomposition

Sudnitsõn, Aleksander; Devadze, Sergei Proceedings of the IEEE East-West Design & Test Workshop (EWDWTW'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 241-246 : ill

Computer engineering

Sudnitsõn, Aleksander PhD in computer science, computer engineering, software engineering, information systems 2007 / p. 121-192

Computing sorted subsets for data processing in communicating software/hardware control systems

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** International journal of computers communications & control 2016 / p. 126-141 : ill <https://doi.org/10.15837/ijccc.2016.1.1442> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Cooperation of FPGA-based educational boards and web-based point design tools for research and education

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus IFIP EduTech'09 International Workshop : Florianopolis-Brazil, October 15-16, 2009 2009 / ? p

A decomposition procedure for register-transfer level power management

Fomina, Jelena; Keevallik, Andres; Kruus, Margus; Sudnitsõn, Aleksander Proceedings of the International Conference on Computer Systems and Technologies (e-Learning) : CompSysTech'2003 : Sofia, Bulgaria, 19-20 June 2003 / p. 1.2-1 - 1.2-6
https://www.researchgate.net/publication/242107053_A_Decomposition_Procedure_for_Register-Transfer_Level_Power_Management

Decompositional synthesis of control-dominated devices for power minimization

Kasirova, Lilia; Keevallik, Andres; Sudnitsõn, Aleksander Mixed design of integrated circuits and systems : proceedings of the 3rd Advanced Training Course : Mixed Design of Integrated Circuits and Systems - Education of Computer Aided Design of Modern ICs and Devices, MIXDES'96, Lodz, Poland, 30 May-1 June 1996 1996 / p. 189-194: ill

Decompositional synthesis of low power controllers

Kasirova, Lilia; Keevallik, Andres; Sudnitsõn, Aleksander BEC'96 : the 5th Biennial Baltic Electronics Conference, October 7-11, 1996, Tallinn, Estonia : proceedings 1996 / p. 191-194: ill

Design of FPGA-based circuits using hierarchical finite state machines

Skliarova, Iouliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** 2012 http://www.ester.ee/record=b2857138*est

Design space exploration in multi-level computing systems

Sklyarov, Valery; Skliarova, Iouliia; Silva, João; **Sudnitsõn, Aleksander** CompSysTech'14 : 15th International Conference on Computer Systems and Technologies : Ruse, Bulgaria, June 27-28, 2014 2014 / p. 40-47 : ill <https://doi.org/10.1145/2659532.2659616>
[Conference proceedings at Scopus](#) [Article at Scopus](#)

Digital design at microarch[itectural] level based on quality relationship measures

Kruus, Margus; Lensen, Harri; Sudnitsõn, Aleksander Успехи современного естествознания 2004 / 5, приложение 1, Материалы XXXI международной конференции и дискуссионного научного клуба : информационные технологии в науке, образовании, телекоммуникации и бизнесе : IT+SE'2004 : Украина, Крым, Ялта-Гурзуф, 18-27 мая 2004 года, с. 29-30

Digital design learning system based on Java applets

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes 4th Annual Conference of the LTSN Centre for Information and Computer Sciences : 26th-28th August 2002, NUI Galway, Ireland 2003 / p. 183-187 : ill
<https://pld.ttu.ee/dlids/publications/Sudnitson%20LTSN-ICS%202003.pdf>

Digital synthesis tools for education and research

Fomina, Jelena; Ellervee, Peeter; Kruus, Margus; Sudnitsõn, Aleksander; Tammemäe, Kalle Proc. 18th International Conference on Systems for Automation of Engineering and Research (SAER'2004) 2004 / p. 160-164

DILOS - автоматизированная система декомпозиционного синтеза и верификации дискретных управляющих устройств

Kruus, Margus; Keevallik, Andres; Berkman, Boriss; Sudnitsõn, Aleksander Внедрение новых информационных технологий в процесс обучени профессионально-технических учебных заведений стран - членов СЭВ 1989 / с. ?

DILOS - интеративная система декомпозиционного логического синтеза

Berkman, Boriss; Keevallik, Andres; Sudnitsõn, Aleksander Тезисы докладов XXX всесоюзной школы-семинара им. М.А. Гаврилова "Развитие теории дискретных систем и проблемы логического проектирования СБИС" (27 июня - 3 июля 1988 г.) 1988 / с. 3

Distance-learning tools for digital design and test issues

Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes IT+SE'2002 : Information Tec[h]nologies in Science, Education, Telecommunication, Business : proceedings = Информационные технологии в науке, образовании, телекоммуникации, бизнесе, Украина, Крым, Ялта-Гурзуф, 20-30 мая 2002 года : труды 2002 / p. 269-272 : ill

E-learning environment in the area of digital microelectronics

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich ITHET 2004 : proceedings of the Fifth International Conference on Information Technology based Higher Education and Training : 31 May - 2 June, 2004, Istanbul, Turkey 2004 / p. 278-283 : ill

E-learning tools for teaching the decomposition based digital synthesis

Sudnitsõn, Aleksander; Kruus, Margus EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 63-66 https://pld.ttu.ee/~kruus/EWME_06_sudn.pdf

E-learning tools for teaching the design and validation of "Finite state machines"

Wuttke, Heinz-Dietrich; **Sudnitsõn, Aleksander**; Henke, Karsten E-learning II and the Knowledge Society with Section for PhD Students in Computing : Communication & Cognition : Ghent, Belgium 2006 / p. 327-341 : ill

Energy reduction techniques at register transfer level synthesis

Sudnitsõn, Aleksander Proc. 16th International Conference on Systems for Automation of Engineering and Research (SAER'2002), Varna, Bulgaria 2002 / p. 48-52

Entropic analysis of finite state mashines' networks

Fomina, Jelena; Keevallik, Andres; Sudnitsõn, Aleksander IEEE Design and Diagnostics of Electronic Circuits and Systems : Fifth International Workshop IEEE DDECS 2002, Brno, Czech Republic, April 17-19, 2002 : proceedings 2002 / p. 244-251 : ill

European thematic network for doctoral education in computing

Smrikarov, A.; Smrikarova, S.; **Kruus, Margus; Sudnitsõn, Aleksander** Материалы XXXIII международной конференции и IV международной конференции молодых ученых : информационные технологии в науке, образовании, телекоммуникации и бизнесе = Information Technologies in Science, Education, Telecommunication and Business : IT+SAMPE'06 : майская сессия : Украина, Крым, Ялта-Гурзуф, 20-30 мая 2006 г 2006 / p. 339-340

Extended finite state machine decomposition for low power

Fomina, Jelena; Sudnitsõn, Aleksander Proceedings 19th International Conference on Systems for Automation of Engineering and Research : SAER'2005 : Varna, Bulgaria, 2005 2005 / p. 126-131

Fast data sort based on searching networks with ring pipeline

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2016 / p. 58-62 : ill <https://doi.org/10.5755/j01.eie.22.4.15920> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast iterative circuits and RAM-based mergers to accelerate data sort in software/hardware systems

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Proceedings of the Estonian Academy of Sciences 2017 / p. 323-335 : ill <https://doi.org/10.3176/proc.2017.3.07> http://www.ester.ee/record=b2355998*est [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast matrix covering in all programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2014 / p. 150-153 : ill <https://doi.org/10.5755/j01.eie.20.5.7116> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fast processing of non-repeated values in hardware

Skliarova, Iuliia; Sklyarov, Valery; **Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2017 / p. 74-77 : ill <https://doi.org/10.5755/j01.eie.23.3.18336> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Fault simulation and code coverage analysis of RTL designs using high-level decision diagrams = Rikete simuleerimine ja koodikatte analüüs register-siirde tasemel kasutades kõrgtaseme otsustusdiagramme

Reinsalu, Uljana 2013 https://www.ester.ee/record=b2963595*est

Finite state machine synthesis for low power using input-disabling precomputation architectures

Sudnitsõn, Aleksander The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 137-140 : ill

Finite state machines with datapath partitioning for low power synthesis

Sudnitsõn, Aleksander Proceedings of the 8th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2001 : Zakopane, Poland, 21-23 June 2000 2001 / p. 163-168 : ill

FPGA platform based digital design education

Mihhailov, Dmitri; Kruus, Margus; Sudnitsõn, Aleksander Proceedings of the 9th International Conference on Computer Systems and Technologies and Workshop for PhD Students in Computing : CompSysTech'2008. Vol. 374, ACM International Conference Proceeding Series 2008 / p. IV.4-1 - IV.4-6 : ill <https://dl.acm.org/doi/pdf/10.1145/1500879.1500938>

FPGA-based accelerators for parallel data sort

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Applied computer systems 2014 / p. 53-63 : ill

FPGA-based systems in information and communication

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** AICT2011 : 5th International Conference on Application of Information and Communication Technologies : 12-14 October, Baku, Azerbaijan : conference proceedings 2011 / p. 551-555 https://www.researchgate.net/publication/254014990_FPGA-based_systems_in_information_and_communication

FPGA-based time and cost effective Hamming weight comparators for binary vectors

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander; Kruus, Margus** Proceedings : EUROCON 2015 : Salamanca, Spain, 8th-11th September 2015 / p. 328-333 : ill <http://dx.doi.org/10.1109/EUROCON.2015.7313700>

A FSM decomposition method for mixed synchronous/asynchronous implementation

Sudnitsõn, Aleksander; Jamšanov, A. Proceedings of the 17th International Conference on Systems for Automation of Engineering and Research : SAER'2003 : Varna, Bulgaria, 2003 2003 / p. 37-41

FSM decomposition software for education and research

Devadze, Sergei; Sudnitsõn, Aleksander Proc. IEEE EUROCON 2005 International Conference on Computer as a tool : Belgrade, Serbia & Montenegro 2005 / p. 839-842 <https://ieeexplore.ieee.org/document/1630063>

FSM decomposition with application to FPGA synthesis

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus; Tarletski, Konstantin International Conference on Computer Systems and Technologies - CompSysTech'09 : Ruse, Bulgaria 2009 / p. IV.4.1-IV.4.6 <https://dl.acm.org/doi/10.1145/1731740.1731820>

FSM's network encoding guided by information relationship measure

Fomina, Jelena; Sudnitsõn, Aleksander; Vasiliev, Roman Boolean Problems : 6th International Workshop : September 23-24, 2004, Freiberg 2004 / p. 55-62

Functional partitioning for register transfer level low power synthesis

Sudnitsõn, Aleksander ECS'01 : proceedings of the 3rd Electronic Circuits and Systems Conference : September 5-7, 2001, Bratislava, Slovakia 2001 / p. 73-76 : ill

Hardware accelerators for information retrieval and data mining

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; **Sudnitsõn, Aleksander; Rjabov, Artjom** 2015 International Conference on Information and Communication Technology Research (ICTRC2015) : Abu Dhabi, United Arab Emirates, May 17-19, 2015 2015 / p. 202-205 : ill <http://dx.doi.org/10.1109/ICTRC.2015.7156457>

Hardware implementation of recursive algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 53rd IEEE International Midwest Symposium on Circuits and Systems : Seattle, Washington, USA, August 1-4, 2010 : proceedings 2010 / p. 225-228 <https://ieeexplore.ieee.org/document/5548674>

Hardware implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA) : Kuala Lumpur, Malaysia, April 25-27, 2011 : [proceedings] 2011 / p. 33-38 : ill <https://ieeexplore.ieee.org/document/5959040>

Hardware implementation of recursive sorting algorithms using tree-like structures and HFSM models = Rekursiivsete sortimisalgoritmid riistvaraline realiseerimine kasutades puulaadseid struktuure ja HFSM mudeleid

Mihhailov, Dmitri 2011 https://www.ester.ee/record=b2748823*est

Hardware/software co-design for programmable systems-on-chip

Sklyarov, Valery; Skliarova, Iuliia; Silva, João; Rjabov, Artjom; **Sudnitsõn, Aleksander;** Cardoso, Cláudia 2014 http://www.ester.ee/record=b3087107*est

Hardware/software co-design in extensible processing platforms for combinatorial search algorithms

Skliarova, Iuliia; Sklyarov, Valery; **Rjabov, Artjom; Sudnitsõn, Aleksander** MELECON 2014 : 2014 17th IEEE Mediterranean Electrotechnical Conference : 13-16 April 2014, Beirut, Lebanon 2014 / p. 462-466 : ill <https://doi.org/10.1109/MELCON.2014.6820578>
[Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

High-performance hardware accelerators for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 313-318 : ill <https://ieeexplore.ieee.org/document/5783103>

High-performance information processing in distributed computing systems

Sklyarov, Valery; **Rjabov, Artjom;** Skliarova, Iuliia; **Sudnitsõn, Aleksander** International journal of innovative computing, information and control 2016 / p. 139-160 : ill https://www.researchgate.net/publication/297047447_High-performance_information_processing_in_distributed_computing_systems [Journal metrics at Scopus](#) [Article at Scopus](#)

Implementation in FPGA of address-based data sorting

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 21st International Conference on Field Programmable Logic and Applications : FPL 2011 : Chania, Crete, Greece, 5-7 September 2011 2011 / p. 405-410 : ill https://www.researchgate.net/publication/220760392_Implementation_in_FPGA_of_Address-Based_Data_Sorting

Implementation of address-based data sorting on different FPGA platforms

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14-17, 2012 2012 / p. 38-41 <https://www.semanticscholar.org/paper/Implementation-of-address-based-data-sorting-on-Mihhailov-Sudnitsõn/e9294d725ab92a2d2a51ccb44fc47e80798bc071>

Implementation of parallel operations over streams in extensible processing platforms

Sklyarov, Valery; Skliarova, Iuliia; **Rjabov, Artjom; Sudnitsõn, Aleksander** 2013 IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS) : August 4-7, 2013, Columbus, Ohio : [proceedings] 2013 / p. 852-855 : ill <https://doi.org/10.1109/MWSCAS.2013.6674783> [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Implementation of sorting algorithms in reconfigurable hardware

Skliarova, Iuliia; Sklyarov, Valery; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2012 IEEE Mediterranean Electrotechnical Conference (MELECON 2012) : Yasmine Hammamet, Tunisia, March 25-28, 2012 / p. 107-110 : ill
<https://ieeexplore.ieee.org/document/6196391>

Information relationships for decomposition of finite state machine

Fomina, Jelena; Sudnitsõn, Aleksander Proceedings of East-West Design & Test Workshop (EWDTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 / p. 41-47

Integrating dynamic power management in the register transfer level synthesis

Sudnitsõn, Aleksander MEET/MARIND'2002 : proceedings of First International Congress on Mechanical and Electrical Engineering and Technology and Fourth International Conference on Marine Industry, 07-11 October 2002, Varna Bulgaria. Volume 1 2002 / p. 267-274 : ill

Integration of high-level synthesis to the courses on reconfigurable digital systems

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander; Kruus, Margus** 2015 38th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO) : May 25-29, 2015, Opatija, Croatia : proceedings 2015 / p. 166-171 : ill <http://dx.doi.org/10.1109/MIPRO.2015.7160258>

Interactions of Zynq-7000 devices with general purpose computers through PCI-express : a case study [Electronic resource]

Rjabov, Artjom; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Proceedings of the 18th Mediterranean Electrotechnical Conference MELECON 2016 : 18-20 April 2016, Limassol, Cyprus 2016 / [4] p. : ill. [CD-ROM]
<https://doi.org/10.1109/MELCON.2016.7495400>

Java applets support for an asynchronous-mode learning of digital design and test

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich ITHET 2003 proceedings : 4th International Conference on Information Technology Based Higher Education and Training : July 7-9, 2003, Marrakech, Morocco 2003 / p. 397-401 : ill <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=92f0b0e5011a2192d5a1b98baa751cb8cd2f7ff3>

Java technology based training system for teaching digital design and test

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 283-286 : ill

Java-based system for finite state machine decomposition

Sudnitsõn, Aleksander; Levenko, Aleksei; Andreev, Dmitri 45. Internationales Wissenschaftliches Kolloquium, 04.-06.10.2000 : Tagungsband 2000 / S. 961-965 : ill

Low power finite state machine synthesis

Fomina, Jelena 2005 https://www.ester.ee/record=b2097121*est

Low power state assignment using ILP techniques

Sagahyroon, Assim; Aloul, Fadi; **Sudnitsõn, Aleksander** The 15th IEEE Mediterranean Electrotechnical Conference – MELCON-2010. Valletta, Malta, April 25-28, 2010 / p. 850-855 http://www.aloul.net/Papers/faloul_power_melecon10.pdf

Low power synthesis based on information theoretic measures

Fomina, Jelena; Keevallik, Andres; Sudnitsõn, Aleksander 23rd International Conference on Microelectronics : MIEL 2002, Niš, Yugoslavia, 12-15 May 2002 : proceedings 2002 / p. 699-702 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=1003354>

Methodology and international collaboration in teaching reconfigurable systems

Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** The 2012 IEEE Global Engineering Education Conference (IEEE EDUCON 2012), Marrakesh, Morocco, Apr. 17-20, 2012 / p. 1143-1152 : ill
https://www.researchgate.net/publication/254034783_Methodology_and_international_collaboration_in_teaching_reconfigurable_systems

Multilevel models for data processing

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE GCC Conference and Exhibition (GCC) : February 19-22, 2011, Dubai, United Arab Emirates 2011 / p. 136-139

Network-based hardware accelerators for parallel data processing = Võrgupõhised riistvarakiirendid paralleelseks andmetöötluseks

Rjabov, Artjom 2017 <https://digi.lib.ttu.ee/i/?8436> https://www.ester.ee/record=b4685402*est

A new approach to state encoding of low power FSM

Fomina, Jelena; Brik, Marina; Sudnitsõn, Aleksander; Vasiliev, Roman Proceedings of IEEE East-West Design & Test Workshop : EWDTW'05 : Ukraine 2005 / p. 21-26

Optimization of address-based data sorting unit with external memory support

Mihhailov, Dmitri; Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** CompSysTech'13 : proceedings of the 14th International Conference on Computer Systems and Technologies 2013 / p. 83-90 : ill <https://doi.org/10.1145/2516775.2516807>
[Conference Proceedings at Scopus](#) [Article at Scopus](#)

Optimization of FPGA-based circuits for recursive data sorting

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 129-132 : ill

Optimization of FSMs network by new encoding strategy

Fomina, Jelena; Sudnitsõn, Aleksander; Vasiliev, Roman BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 119-122 : ill

Optimization of recursive sorting algorithms for implementation in hardware

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Proceedings of 22nd International Conference on Microelectronics (ICM 2010) : Cairo, Egypt, Dec. 19-22, 2010 2010 / p. 471-474 : ill
https://www.researchgate.net/publication/224213497_Optimization_of_recursive_sorting_algorithms_for_implementation_in_hardware

Parallel FPGA-based implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 121-126 : ill
https://www.researchgate.net/publication/221437230_Parallel_FPGA-Based_Implementation_of_Recursive_Sorting_Algorithms

Partition search for FSM low power synthesis

Sudnitsõn, Aleksander Proceedings of the 4th International Conference "Computer-Aided Design of Discrete Devices" : CAD DD'2001 : Minsk, Belarus, 2001. Vol. 1 2001 / p. 44-49

Partition search problem for finite state machine decomposition

Sudnitsõn, Aleksander 45. Internationales Wissenschaftliches Kolloquium, 04.-06.10.2000 : Tagungsband 2000 / S. 673-678 : III

Performance evaluation for FPGA-based processing of tree-like structures

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 19th IEEE International Conference on Electronics, Circuits, and Systems (IEEE ICECS), Sevilla, Spain, December 9-12, 2012 2012 / p. 217-220 : ill
<https://ieeexplore.ieee.org/document/6463762>

Processing N-ary trees in hardware circuits

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 13th International Symposium on Integrated Circuits (ISIC) : Singapore, 12-14 December 2011 : proceedings 2011 / p. 262-265 : ill <https://ieeexplore.ieee.org/document/6131946>

Processing N-ary trees in reconfigurable hardware

Sklyarov, Valery; Skliarova, Iuliia; Sudnitsõn, Aleksander 2013 25th International Conference on Microelectronics (ICM) : 15-18 December 2013, Beirut-Lebanon 2013 / p. 13-16 : ill

Processing sorted subsets in a multi-level reconfigurable computing system

Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Elektronika ir elektrotehnika = Electronics and electrical engineering 2015 / p. 30-33 : ill <https://doi.org/10.5755/j01.eee.21.2.11509> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Processing tree-like data structures for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE Symposium on Computers & Informatics : ISC12011 : Kuala Lumpur, Malaysia, 20-23 March 2011 2011 / p. 322-327
https://www.researchgate.net/publication/252020117_Processing_tree-like_data_structures_for_sorting_and_managing_priorities

Processing tree-like data structures in different computing platforms

Sklyarov, Valery; Skliarova, Iuliia; Oliveira, Ramiro; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 International Conference on Information and Computer Applications (ICICA 2011) : Dubai, United Arab Emirates, March 18-20, 2011 2011 / p. 112-116 : ill
https://sweet.ua.pt/iouliia/Papers/2011/rp025_ICICA2011-A067.pdf

Professional standards and curricula of doctoral education in computer engineering

Kruus, Margus; Viies, Vladimir; Sudnitsõn, Aleksander Труды XXXV юбилейной международной конференции. VI международная конференция молодых ученых : информационные технологии в науке, образовании, телекоммуникации и бизнесе : IT+SAMPE'08 : майская сессия : Украина, Крым, Ялта-Гурзуф, 20-30 мая, 2008 г 2008 / p. 302-303

Project-oriented approach to low-power topics in advanced digital design course

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Kruus, Margus Elektronika ir elektrotehnika = Electronics and electrical engineering 2010 / 6, p. 151-154 <https://eejournal.ktu.lt/index.php/elt/article/view/9381>

RAM-based mergers for data sort and frequent item computation [Electronic resource]

Rjabov, Artjom; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** 2017 40th International Convention on Information and Communication Technology, Electronics and Microelectronics (MIPRO), May 22 - 26, 2017, Opatija, Croatia : proceedings 2017 / p. 176-181 : ill. [CD-ROM] <http://dx.doi.org/10.23919/MIPRO.2017.7973413>

Reconfigurable systems in engineering education : best practices and future trends

Skliarova, Ioulia; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** Proceedings of 2017 IEEE Global Engineering Education Conference (EDUCON) : 25-28 April 2017, Athens, Greece 2017 / p. 1084-1088 : ill
<https://doi.org/10.1109/EDUCON.2017.7942983>

Recursion and hierarchy in digital design and prototyping : a case study

Mihhailov, Dmitri; Kruus, Margus; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill
<https://dl.acm.org/doi/pdf/10.1145/2023607.2023616>

Register transfer low power design based on controller decomposition

Sudnitsõn, Aleksander MIEL 2004 : 24th International Conference on Microelectronics : Niš, Serbia and Montenegro, 16-19 May 2004 : proceedings. Volume 2 2004 / p. 735-738 : ill <https://ieeexplore.ieee.org/document/1314937>

Research and training environment for decomposition-based logical design

Sudnitsõn, Aleksander E-learning and the Knowledge Society : Communication & Cognition : Ghent, Belgium 2005 / ? p

Software environment for synthesis of testable FSM through decomposition

Devadze, Sergei; Sudnitsõn, Aleksander 2008 26th International Conference on Microelectronics (MIEL 2008) : proceedings 2008 / p. 433-436 <https://ieeexplore.ieee.org/document/4559314>

Solving computationally intensive problems in reconfigurable hardware : a case study

Skliarova, Ioulia; Vallejo, Tiago; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** Journal of convergence information technology (JCIT) : an international journal 2013 / p. 601-609 : ill

Synthesis and implementation of hierarchical finite state machines with implicit modules

Sklyarov, Valery; Skliarova, Ioulia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 436-441 : ill
https://www.researchgate.net/publication/221437255_Synthesis_and_Implementation_of_Hierarchical_Finite_State_Machines_with_Implicit_Modules

Synthesis of sequential circuits with dynamic power management

Lensen, Harri; Kruus, Margus; Sudnitsõn, Aleksander Proc. of 42nd International Scientific Conference of Riga Technical University : RTUCET'01 2001 / p. 81-86

Synthesis of sequential circuits with dynamic power management

Lensen, Harri; Kruus, Margus; Sudnitsõn, Aleksander Scientific proceedings of Riga Technical University. 7.seriija, Telecommunications and electronics 2001 / p. 81-86

Synthesis of testable FSM through decomposition

Devadze, Sergei; Sudnitsõn, Aleksander Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 101-104 : ill

A system for teaching basic and advanced topics of IEEE 1149.1 boundary scan standard (extended abstract)

Jutman, Artur; Rosin, Vjatšeslav; **Sudnitsõn, Aleksander; Ubar, Raimund-Johannes;** Wuttke, Heinz-Dietrich Proceedings of 16th EAEEIE Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Lappeenranta, Finland, 6th-8th June 2005 2005 / [2] p. : ill

Zynq-based system for extracting sorted subsets from large data sets

Sklyarov, Valery; Skliarova, Ioulia; **Rjabov, Artjom; Sudnitsõn, Aleksander** Journal of microelectronics, electronic components and materials 2015 / p. 142-152 : ill <https://ojs.midem-drustvo.si/index.php/InfMIDEM/article/view/117/0> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Teaching digital RT-level self-test using a Java applet

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich 20th IEEE NORCHIP Conference : Copenhagen, Denmark, November 11-12, 2002 2002 / p. 322-328 : ill

Teaching FPGA-based systems

Skliarova, Ioulia; Sklyarov, Valery; **Sudnitsõn, Aleksander; Kruus, Margus** 2014 IEEE Global Engineering Education Conference (EDUCON) : Istanbul, Turkey, April 2-5, 2014 2014 / p. 460-469 : ill

Transforming VHDL descriptions from behavior to structure

Berkman, Boriss; Sudnitsõn, Aleksander; Udre, Jüri Tallinna Tehnikaülikooli Toimetised 1990 / lk. 27-44 : ill

Using mobile technology to enhance teaching reconfigurable systems

Skliarova, Iuliia; Sklyarov, Valery; Sudnitsõn, Aleksander; Kruus, Margus Proceedings of 2013 IEEE International Conference on Teaching, Assessment and Learning for Engineering (TALE) 2013 / p. 478-483 : ill

Using SAT-based techniques in low power state assignment

Sagahyroon, Assim; Aloul, Fadi; Sudnitsõn, Aleksander Journal of circuits, systems, and computers 2011 / p. 1605-1618 : ill
<https://www.worldscientific.com/doi/10.1142/S0218126611007980>

Web based tools for synthesis and testing of digital devices

Devadze, Sergei; Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the International Conference on Computer Systems and Technologies (e-Learning) : CompSysTech'2002, Sofia, Bulgaria, 20-21 June 2002 / p. 1.9-1 - 1.9-6 : ill
https://www.researchgate.net/publication/250738271_Web_Based_Tools_for_Synthesis_and_Testing_of_Digital_Devices

Web-based applet for teaching boundary scan standard IEEE 1149.1

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the 10th International Conference : Mixed Design of Integrated Circuits and Systems : MIXDES 2003 : Lodz, Poland, 26-28 June 2003 2003 / p. 584-589 : ill
<https://www.semanticscholar.org/paper/WEB-BASED-APPLET-FOR-TEACHING-BOUNDARY-SCAN-IEEE-.-J.-Utman/3bd1b47848612e44772b4c84a2913c419de940fa>

Web-based computer aided design support of finite state machine additive decomposition for low power

Sudnitsõn, Aleksander; Devadze, Sergei 5th IEEE East-West Design & Test International Symposium 2007 / p. 494-498

Web-based software implementation of finite state machine decomposition for design and education

Devadze, Sergei; Kruus, Margus; Sudnitsõn, Aleksander CompSysTech' 2001 : proceedings of the International Conference on Computer Systems and Technologies, Sofia, 21-22 June 2001 2001 / [6] p. : ill
https://pld.ttu.ee/decomposition/publications/Sudnitson_CST_Estonia.pdf

Web-based software package for e-learning and research training in digital system design

Jutman, Artur; Kruus, Margus; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes; Wuttke, Heinz-Dietrich Информационные технологии в науке, образовании, телекоммуникации и бизнесе : Материалы XXXII Международной конференции IT+SE'2005 : Украина, Крым, Ялта-Гурзуф, 19-28 мая 2005 г 2005 / [2] p

Web-based system for sequential machines decomposition

Devadze, Sergei; Fomina, Jelena; Kruus, Margus; Sudnitsõn, Aleksander The IEEE Region 8 EUROCON 2003 : Computer as a Tool : 22-24. September 2003, Ljubljana, Slovenia : proceedings. Volume A 2003 / p. 57-61 : ill
https://pld.ttu.ee/decomposition/publications/Sudnitson-EUROCON_v5%20_1_.pdf

Web-based tool for FSM encoding targeting low-power FPGA implementation

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Tarletski, Konstantin 2010 27th International Conference on Microelectronics : MIEL 2010 : Niš, Serbia, 16-19 May 2010 : proceedings 2010 / p. 349-352 <https://ieeexplore.ieee.org/document/5490468>

Web-based tools for decomposition-oriented digital design

Kruus, Margus; Lensen, Harri; Sudnitsõn, Aleksander MEET/MARIND'2002 : proceedings of First International Congress on Mechanical and Electrical Engineering and Technology and Fourth International Conference on Marine Industry, 07-11 October 2002, Varna Bulgaria. Volume 1 2002 / p. 261-266 : ill

Web-based tools for finite state machine decomposition with analysis of information flows

Fomina, Jelena; Keevallik, Andres; Kruus, Margus; Sudnitsõn, Aleksander BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 165-168 : ill

Web-based training system for teaching basics of RT-level digital design, test, and design for test [Electronic resource]

Devadze, Sergei; Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes 9th International Conference MIXDES 2002 : Mixed Design of Integrated Circuits and Systems, Wroclaw, Poland, 20-22 June 2002 2002 / [6] p. : ill. [CD-ROM]

Web-based training system for teaching principles of boundary scan technique

Jutman, Artur; Sudnitsõn, Aleksander; Ubar, Raimund-Johannes Proceedings of the 14th EIEEE Annual International Conference on Innovation in Education for Electrical and Information Engineering (EIE) : Gdansk, Poland, 2003 2003 / p. 1-6 : ill

Virtual European department of computing project : problems and perspectives

Kruus, Margus; Sudnitsõn, Aleksander Материалы XXX юбилейной международной конференции и международной конференции молодых ученых : Информационные технологии в науке, образовании, телекоммуникации и бизнесе = Information Technologies in Science, Education, Telecommunication and Business : IT + SE'2003 : Украина, Крым, Ялта-Гурзуф, 19-28 мая 2003 года 2003 / p. 280-283

Генерация псевдослучайного микропрограммного автомата

Sudnitsõn, Aleksander; Berkman, Boriss Автоматизация логического проектирования : сборник научных трудов 1981 / с. 144-152 https://www.ester.ee/record=b1550042*est

Декомпозиционный синтез управляющих автоматов на программируемых матрицах и микропроцессорах : автореферат ... кандидата технических наук (05.13.01)

Sudnitsõn, Aleksander 1983 https://www.ester.ee/record=b1291157*est

Декомпозиционный синтез управляющих автоматов на программируемых матрицах и микропроцессорах : диссертация на соискание ученой степени кандидата кандидата технических наук

Sudnitsõn, Aleksander 1983 https://www.ester.ee/record=b4634419*est

Декомпозиция микропрограммных автоматов на микропроцессоры

Keevallik, Andres; Sudnitsõn, Aleksander Синтез управляющих устройств на основе микропроцессов и однородных сред : труды II всесоюзного семинара, Рязань, дек. 1979 г. 1980 / с. 16-20 https://www.ester.ee/record=b2632002*est

Декомпозиция микропрограммных автоматов с разделением входных переменных

Berkman, Boriss; Sudnitsõn, Aleksander XXV студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 21-23 апреля 1981 года : тезисы докладов. Том 2, Автоматика. Энергетика. Механика. Химия 1981 / с. 30 https://www.ester.ee/record=b1322629*est

Декомпозиция микропрограммных автоматов с разделением выходных переменных

Sudnitsõn, Aleksander Методы синтеза и диагностирования цифровых схем 1985 / с. 13-18
https://www.ester.ee/record=b1302568*est <https://digikogu.taltech.ee/et/Item/e00f2c15-fd8c-48ac-9963-76da1d62d592>

Задача выбора разбиений в декомпозиционном синтезе дискретных управляющих автоматов

Sudnitsõn, Aleksander; Viies, Vladimir Машинное проектирование электронных устройств и систем 1986 / с. 18-28

К вопросу повышения эффективности преподавания основ программирования

Leis, Paul; Sudnitsõn, Aleksander Актуальные вопросы математики, информатики и вычислительной техники в учебном процессе школы и педвуза 1987 / с. 30-31

К проблеме построения сетей микро-ЭВМ для реализации алгоритмов управления

Eledin, V.; Sudnitsõn, Aleksander; Tomilov, V. XXV студенческая научно-техническая конференция вузов Прибалтийских республик, Белорусской ССР и Молдавской ССР, 21-23 апреля 1981 года : тезисы докладов. Том 2, Автоматика. Энергетика. Механика. Химия 1981 / с. 31 https://www.ester.ee/record=b1322629*est

К решению задачи общей декомпозиции конечных автоматов

Sudnitsõn, Aleksander Ускорение внедрения методов и средств автоматизации проектирования и улучшения подготовки специалистов : Тезисы докладов научно-практические конференции молодых ученых и специалистов (г. Гродно, 18-19 окт. 1978 г.) 1978 / с. 156-157

Метод декомпозиции конечных автоматов с использованием алгебры пар покрытий

Sudnitsõn, Aleksander Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 3-9
https://www.ester.ee/record=b1281890*est <https://digikogu.taltech.ee/et/Item/8e0abfe2-9020-4ebd-85d1-fd67de0d1b30>

Метод декомпозиции микропрограммных автоматов с учетом ограничений на число входных переменных

Leis, Paul; Sudnitsõn, Aleksander Расчет и проектирование приборов, устройств и систем технической кибернетики 1980 / с. 41-47 https://www.ester.ee/record=b1264145*est <https://digikogu.taltech.ee/et/Item/81bf2178-a9f8-417d-86c7-2000cca6a01e>

Метод программной реализации микропрограммного автомата

Keevallik, Andres; Kitsnik, Peeter; Sudnitsõn, Aleksander Расчет и проектирование систем технической кибернетики 1983 / с. 91-96 : ил https://www.ester.ee/record=b1288991*est <https://digikogu.taltech.ee/et/Item/7d7515af-76b7-4d35-89a7-e80367d5b635>

Микропроцессорная измерительная станция мониторинга с перенастраиваемой структурой

Viies, Vladimir; Mikhelsen, R.; Sudnitsõn, Aleksander Охрана окружающей среды от загрязнения промышленными выбросами ЦБП : Межвузовский сборник научных трудов 1988 / с. 5

Микропроцессорные системы : учебно-методическое пособие

1983 https://www.ester.ee/record=b1241140*est

Один метод декомпозиционного синтеза микропрограммных автоматов на программируемых логических матрицах

Leis, Paul; Sudnitsõn, Aleksander Труды пятого Международного семинара "Прикладные аспекты теории автоматов". Т. 1 1979 / с. 253-262

Один подход к автоматизации проектирования микропроцессорных систем дискретного управления

Keevallik, Andres; Berkman, Boriss; Sudnitsõn, Aleksander Микропроцессорные системы обработки информации и управления : тезисы докладов 1987 / с. ?

Применение методов декомпозиции конечных автоматов для построения сетей микропроцессоров

Keevallik, Andres; Sudnitsõn, Aleksander Синтез управляющих устройств на основе микропроцессов и однородных сред : труды II всесоюзного семинара, Рязань, дек. 1979 г. 1980 / с. [?] https://www.ester.ee/record=b2632002*est

Реализация сетей автоматов на микропроцессорных БИС

Sudnitsõn, Aleksander; Berkman, Boriss Расчет и проектирование систем технической кибернетики 1984 / с. 45-56 : ил https://www.ester.ee/record=b1549179*est <https://digikogu.taltech.ee/et/Item/99cc4681-4aa3-466a-b6da-b76f575d0f1e>

САПР дискретных систем программно-логического управления

Berkman, Boriss; Keevallik, Andres; Sudnitsõn, Aleksander Международная конференция "Проблемы автоматизированного проектирования в машиностроении "САПР-88", 21-25 марта 1988 г., Москва : Тезисы докладов 1988 / с. ?

Синтез коммутаторов на основе ПЛМ для микропроцессоров, реализующих наборы крупных операций

Božič, V.I.; Galujev, G.A.; **Sudnitsõn, Aleksander** Синтез и диагностика цифровых устройств и систем 1982 / с. 85-91 : ил https://www.ester.ee/record=b1328194*est <https://digikogu.taltech.ee/et/Item/febd586e-d7fa-4fbd-bf41-40576a75f94b>

Синтез мультимикропроцессорных систем дискретного управления

Keevallik, Andres; Sudnitsõn, Aleksander; Berkman, Boriss Тезисы докладов Республиканской научно-технической конференции, посвященной Дню радио, октябрь 1983. Секция "Микропроцессорная техника" 1983 / с. 10-12 https://www.ester.ee/record=b1295287*est

Система автоматизации декомпозиционного синтеза дискретных управляющих устройств (DILOS)

Keevallik, Andres; Sudnitsõn, Aleksander; Berkman, Boriss Методы синтеза и диагностирования цифровых схем 1985 / с. 27-33 : ил https://www.ester.ee/record=b1302568*est <https://digikogu.taltech.ee/et/Item/e00f2c15-fd8c-48ac-9963-76da1d62d592>

Электротехника и автоматика

Rüstern, Ennu; Leis, Paul; Sudnitsõn, Aleksander; Viies, Vladimir; Berkman, Boriss; Keevallik, Andres; Kruus, Margus; Ubar, Raimund-Johannes; Alango, Villem; Kont, Toomas; Grigorjeva, Ksenja; Einasto, N.; Evartson, Teet; Gerasimtšuk, Valeri; Mahhitko, V.P.; Šendrik, M.G.; Tamm, Boris, inform. 1986 https://www.ester.ee/record=b1296477*est