

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation

Leveugle, R.; Ubar, Raimund-Johannes Electron technology 1999 / 3, p. 282-287 : ill

Synthesis of decision diagrams from clock-driven multi-process VHDL descriptions for test generation

Leveugle, R.; Ubar, Raimund-Johannes Proceedings of the 5th International Conference on Mixed Design of Integrated Circuits and Systems, Lodz, Poland, June 18-20, 1998 1998 / p. 353-358