

From virtual characterization to test-chips : DFM analysis through pattern enumeration

Martins, Mayler G.A.; **Pagliarini, Samuel Nascimento**; Isgenc, Mehmet Meric; Pileggi, Larry IEEE transactions on computer-aided design of integrated circuits and systems 2020 / p. 520-532 <https://doi.org/10.1109/TCAD.2018.2889772>

Hardware trojan insertion in finalized layouts : from methodology to a silicon demonstration

Perez, Tiago Diadami; Pagliarini, Samuel Nascimento IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems 2023 / p. 2094-2107 <https://doi.org/10.1109/TCAD.2022.3223846> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

A security-aware and LUT-based CAD flow for the physical synthesis of hASICs

Abideen, Zain Ul; Perez, Tiago Diadami; Martins, Mayler; **Pagliarini, Samuel Nascimento** IEEE transactions on computer-aided design of integrated circuits and systems 2023 / p. 3157-3170 : ill <https://doi.org/10.1109/TCAD.2023.3244879> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

System-level data format exploration for dynamically allocated data structures

Ellervee, Peeter; Miranda, Miguel; Catthoor, Francky; Hemani, Ahmed IEEE transactions on computer-aided design of integrated circuits and systems 2001 / 12, p. 1469-1472 : ill <https://ieeexplore.ieee.org/abstract/document/969440>