

JÄNES : a NAS framework for ML-based EDA applications

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2021 <https://doi.org/10.1109/DFT52944.2021.9568321>

Keynote: cost-efficient reliability for Edge-AI chips

Jenihhin, Maksim; Taheri, Mahdi; Cherezova, Natalia; Ahmadilivani, Mohammad Hasan; Selg, Hardi; Jutman, Artur; Shibin, Konstantin; Tsertov, Anton; Devadze, Sergei; Kodamanchili, Rama Mounika; Rafiq, Ahsan; Raik, Jaan; Daneshtalab, Masoud 2024 IEEE 25th Latin American Test Symposium (LATS) 2024 / 2 p <https://doi.org/10.1109/LATS62223.2024.10534610> [Article at Scopus](#)

ML-based online design error localization for RISC-V implementations

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS) : IOLTS 2023 : July 3rd-5th, 2023, Platanias, Chania (Crete), Greece : proceedings 2023 / 7 p. <https://doi.org/10.1109/IOLTS59296.2023.10224864>

Special session: in-field ML-assisted intermittent fault localization and management in RISC-V SoCs

Selg, Hardi; Shibin, Konstantin; Tsertov, Anton; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2024 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2024 <https://doi.org/10.1109/DFT63277.2024.10753541> [Article at Scopus](#)

Wafer-level die re-test success prediction using machine learning

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter 21st IEEE Latin-American Test Symposium (LATS) 2020 : proceedings 2020 / 5 p <https://doi.org/10.1109/LATS49555.2020.9093672>