

Exploration of Activation Fault Reliability in Quantized Systolic Array-Based DNN Accelerators

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A fault-resistant architecture for AES S-box architecture

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A high-performance MEMRISTOR-based Smith-Waterman DNA sequence alignment using FPN structure

Taheri, Mahdi; Zandevakili, Hamed; Mahani, Ali Journal of Applied Research in Electrical Engineering 2021 / p. 59-68 <https://doi.org/10.22055/jaree.2021.36117.1016>

A novel fault-tolerant logic style with self-checking capability

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