

An approach to system-level design for test

Jervan, Gert; Ubar, Raimund-Johannes; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 121-149 : ill

High-level test synthesis with hierarchical test generation

Jervan, Gert; Eles, Petru; Peng, Zebo; **Raik, Jaan; Ubar, Raimund-Johannes** 17th NORCHIP Conference : Oslo, Norway, 8-9 November 1999 : proceedings 1999 / p. 291-296

Hybrid BIST time minimization for core-based systems with STUMPS architecture

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes; Jenihhin, Maksim** 18th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems : 3-5 November 2003, Boston, Massachusetts : proceedings 2003 / p. 225-232 : ill
<https://ieeexplore.ieee.org/document/1250116>

Power-constrained hybrid BIST test scheduling in an abort-on-first-fail test environment

He, Zhiyuan; **Jervan, Gert;** Peng, Zebo; Eles, Petru Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 83-86 : ill
<https://ieeexplore.ieee.org/document/1559782>

Test generation : a hierarchical approach

Jervan, Gert; Ubar, Raimund-Johannes; Peng, Z.; Eles, Petru System-level test and validation of hardware/software systems 2005 / p. 67-81 : ill

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes; Jenihhin, Maksim** 12th Asian Test Symposium (ATS 2003) : 17-19 November 2003, Xian, China 2003 / p. 318-325 : ill <https://link.springer.com/article/10.1007/s11390-006-0907-x>

Test time minimization for hybrid BIST of core-based systems

Jervan, Gert; Eles, Petru; Peng, Zebo; **Ubar, Raimund-Johannes; Jenihhin, Maksim** Journal of computer science and technology 2006 / 6, p. 907-912 : ill <https://link.springer.com/article/10.1007/s11390-006-0907-x>