

An ad-hoc implementation of a remote laboratory

Azad, Siavoosh Payandeh; Kinks, Hannes; Tajammul, Muhammad Adeel; Ellervee, Peeter 2015 International Conference on Microelectronic Systems Education : MSE '15 : Pittsburgh, PA, May 20-21, 2015 / p. 48-51 : ill
<http://dx.doi.org/10.1109/MSE.2015.7160015>

Analog integrated circuits and signal processing

Ellervee, Peeter; Jervan, Gert 2010

Applying FPGA partial reconfiguration for digital system simulation

Arhipov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 145-148 : ill

Architectural exploration tasks for on-chip embedded systems

Reinsalu, Uljana; Arhipov, Anton; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 171-174 : ill

Architectural solutions for high-speed data processing demands of CERN LHC detectors with FPGA and high-level synthesis

Devadze, Sergei; Nielsen, Christine Elizabeth; Mihhailov, Dmitri; Ellervee, Peeter 2024 IEEE Nordic Circuits and Systems Conference (NorCAS) 2024 <https://doi.org/10.1109/NorCAS64408.2024.10752490> [Article at Scopus](#)

Arvutiteadlaste töötajimustest Rootsi kõrgkoolis

Ellervee, Peeter Arvutustehnika ja Andmetöötlus 1990 / 12, lk. 49-53

At-speed self-testing of high-performance pipe-lined processing architectures [Electronic resource]

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart 31st Norchip Conference : Vilnius, Lithuania, 11-12 November 2013 : conference program and papers 2013 / p. 1-6 : ill [USB]

At-speed testing and test quality evaluation for high-performance pipelined systems Töökiirusel testimine ja testi kvaliteedi hindamine kõrgjõudlus-konveierarhitektuuriga süsteemidele

Gorev, Maksim 2015 <https://digi.lib.ttu.ee/i/73953>

Automatic synthesis of asynchronous circuits from synchronous RTL descriptions

Öberg, Johnny; Plosila, Juha; Ellervee, Peeter Proceedings 23rd NORCHIP Conference : Oulu, Finland, 21-22 November 2005 2005 / p. 200-205 : ill <https://ieeexplore.ieee.org/document/1597024/keywords#keywords>

A benchmark suite for evaluating the efficiency of test tools

Kruus, Helena; Ubar, Raimund-Johannes; Ellervee, Peeter; Gorev, Maksim; Pesonen, Vadim; Devadze, Sergei; Orasson, Elmet; Brik, Marina; Min, Mart; Annus, Paul; Kruus, Margus; Meigas, Kalju BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 85-88 : ill

Bottlenecks in hardware design and design automation [Electronic resource] : [slides]

Ellervee, Peeter Design and Test Technology for Dependable Hardware/Software Systems : DEDIS/DAAD Summer Academy : BTU Cottbus, Sept. 1st-12th, 2008 2008 / [24] p. : ill. [CD-ROM]

Bottlenecks in hardware design and design automation (Hardware synthesis: no pain, no gain)

Ellervee, Peeter CREDES Summer School : Dependable Systems Design : handouts 2011 / p. 49-58 : ill

CLD : an accurate, cost-effective and scalable run-time Cache Leakage Detector

Shalabi, Ameer; Ghasempouri, Tara; Ellervee, Peeter; Raik, Jaan 2021 24th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : Vienna, Austria, 07-09 April 2021 2021 / p. 127-132 : ill
<https://doi.org/10.1109/DDECS52668.2021.9417071>

Clock manipulation for heterogeneous emulation environment

Ellervee, Peeter; Arhipov, Anton; Tammemäe, Kalle Proceedings [of] 24th IEEE Norchip Conference : Linköping, Sweden, 20-21 November 2006 2006 / p. 213-216 : ill <https://ieeexplore.ieee.org/abstract/document/4126984>

Code compaction within CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Ellervee, Peeter Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 133-136 : ill

Code coverage analysis using high-level decision diagrams [Electronic resource]

Raik, Jaan; Reinsalu, Uljana; Ubar, Raimund-Johannes; Jenihhin, Maksim; Ellervee, Peeter 2008 IEEE Design and

Diagnostics of Electronic Circuits and Systems : Bratislava, Slovakia, April 16-18, 2008 2008 / p. 201-207 : ill. [CD-ROM]
<https://ieeexplore.ieee.org/document/4538786>

Communication modelling and synthesis for NoC-based systems with real-time constraints

Tagel, Mihkel; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 237-242 : ill
<https://www.semanticscholar.org/paper/Communication-modelling-and-synthesis-for-NoC-based-Tagel-Ellervee/71f9595d88ed06b63367b87188b218fe6da6bd97>

A comparison of six languages for system level description of telecom applications

Jantsch, Axel; Kumar, Shashi; Sander, Ingo; Svantesson, Bengt; **Öberg, Johnny**; Hemani, Ahmed; **Ellervee, Peeter**; O'Nils, Mattias
Electronic chips & systems design languages 2001 / p. 181-192 : ill https://link.springer.com/chapter/10.1007/978-1-4757-3326-6_15

Contention aware scheduling for NoC-based real-time systems

Tagel, Mihkel; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert Norchip 2011 : 14-15 November 2011, Lund 2011 / [4] p.: ill

Contention aware scheduling for NoC-based real-time systems

Tagel, Mihkel; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 75-78 : ill

Customizable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; **Ellervee, Peeter** 2014 IEEE 22nd International Symposium on Field-Programmable Custom Computing Machines : FCCM 2014 : 11-13 May 2014, Boston, Massachusetts, USA : proceedings 2014 / p. 31 : ill

DAC 2000 - 37th Design Automation Conference

Ellervee, Peeter A & A 2000 / 5, lk. 53-54 https://artiklid.elnet.ee/record=b1005204*est

Data analysis for embedded software performance and energy consumption estimation

Ruberg, Priit; Liiv, Elvar; Lass, Keijo; Ellervee, Peeter 2019 IEEE 2nd Ukraine Conference on Electrical and Computer Engineering : UKRCON-2019 : conference proceedings 2019 / p. 928-933 : ill <https://doi.org/10.1109/UKRCON.2019.8879787>

Data type dependent energy consumption estimation

Ruberg, Priit; Lass, Keijo; Ellervee, Peeter 2nd IEEE NORCAS Conference : 1-2 November 2016, Copenhagen, Denmark 2016 / [5] p. : ill <https://doi.org/10.1109/NORCHIP.2016.7792916>

Dependability evaluation in fault-tolerant systems with high-level decision diagrams

Ubar, Raimund-Johannes; Jervan, Gert; Raik, Jaan; Jenihhin, Maksim; Ellervee, Peeter Computer Science Meets Automation : 10-13 September 2007 : proceedings. Volume II 2007 / p. 147-152 : ill https://www.db-thueringen.de/receive/dbt_mods_00008864

Design space exploration and optimisation for NoC-based timing sensitive systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK neljanda aastakonverentsi artiklite kogumik : 26.-27. novembril 2010, Essu mõis 2010 / lk. 117-120 : ill

Design space exploration and optimisation for NoC-based timing sensitive systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 177-180 : ill

Developing a data acquisition system for measuring microcontroller energy consumption using LabVIEW

Ruberg, Priit; Lass, Keijo; Ellervee, Peeter BEC 2016 : 2016 15th Biennial Baltic Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-5, 2016, Tallinn, Estonia 2016 / p. 123-126 : ill
http://www.ester.ee/record=b2150914*est

Digitaali disain - ideest realiseerimiseni

Ellervee, Peeter A & A 2008 / lk. 6-10 : ill https://artiklid.elnet.ee/record=b1021438*est

Digital electronics design and test at Computer Engineering Department of Tallinn University of Technology

Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Ellervee, Peeter The house magazine : the parliamentary weekly 2006 / 1198, p. 42 : ill

Digital hardware organization course for SoC program

Ellervee, Peeter; Tenhunen, Hannu 2001 International Conference on Microelectronic Systems Education : June 17-18, 2001, Las Vegas, Nevada, USA : proceedings 2001 / p. 26-27 <https://ieeexplore.ieee.org/document/932402>

Digital synthesis tools for education and research

Fomina, Jelena; Ellervee, Peeter; Kruus, Margus; Sudnitsõn, Aleksander; Tammemäe, Kalle Proc. 18th International

Digital system modeling and synthesis as an introduction to computer systems engineering

Tajammul, Muhammad Adeel; Azad, Siavoosh Payandeh; Ellervee, Peeter 2015 International Conference on Microelectronic Systems Education : MSE '15 : Pittsburgh, PA, May 20-21, 2015 2015 / p. 52-55 : ill <http://dx.doi.org/10.1109/MSE.2015.7160016>

DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Ellervee, Peeter; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha 28th International Conference on VLSI Design : held concurrently with 14th International Conference on Embedded Systems : 3-7 January 2015, Bangalore, India : proceedings 2015 / p. 547-552 : ill <https://doi.org/10.1109/VLSID.2015.98> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

DyMeP : an infrastructure to support dynamic memory binding for runtime mapping in CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Ellervee, Peeter; Hemani, Ahmed; Tenhunen, Hannu; Plosila, Juha Doctoral School in Information and Communication Technology : proceedings of doctoral session of BEC 2014 : October 6-8 2014, Laulasmaa 2014 / lk. 19-22 : ill

EEG analyzer prototype based on FPGA

Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Ellervee, Peeter; Hinrikus, Hiie; Bachmann, Maie; Lass, Jaanus 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011) : September 4-6, 2011, Dubrovnik, Croatia : proceedings 2011 / p. 101-106 : ill <https://ieeexplore.ieee.org/document/6046588>

Embedded software performance estimations at different compiler optimisation levels

Ruberg, Priit; Lass, Keijo; Liiv, Elvar; Ellervee, Peeter Advances in Information, Electronic and Electrical Engineering (AIEEE) : proceedings of the 5th IEEE Workshop, november 24-25, 2017, Riga, Latvia 2017 / p. 1-6 : ill <https://doi.org/10.1109/AIEEE.2017.8270530>

Energy consumption and performance estimation of embedded software = Sardtarkvara energiatarbe ja jõudluse ennustamine

Ruberg, Priit 2018 <https://digi.lib.ttu.ee/i/?10704> https://www.ester.ee/record=b5152952*est

Environment for fault simulation acceleration on FPGA

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 217-220 : ill

Environment for FPGA-based fault emulation

Ellervee, Peeter; Raik, Jaan; Tammemäe, Kalle; Ubar, Raimund-Johannes Proceedings of the Estonian Academy of Sciences. Engineering 2006 / 3-2, p. 323-335 : ill

Evaluating fault emulation on FPGA

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin; Tammemäe, Kalle Field-Programmable Logic and Applications : 14th International Conference, FPL 2004 : Antwerp, Belgium, August 30-September 1, 2004 : proceedings 2004 / p. 354-363 : ill https://link.springer.com/chapter/10.1007/978-3-540-30117-2_37

Experience in increase of practical hours for HDL course

Reinsalu, Uljana; Ellervee, Peeter 2011 International Conference on Microelectronic Systems Education (MSE '11), 5-6 June 2011, San Diego, California 2011 / p. 102-105 <https://ieeexplore.ieee.org/document/5937104>

Exploiting data transfer locality in memory mapping

Ellervee, Peeter; Miranda, Miguel; Catthoor, Francky; Hemani, Ahmed 25th EUROMICRO conference : Informatics : Theory and Practice for the New Millennium : Milan, Italy, September 8-10, 1999 : proceedings. Volume I 1999 / p. 14-21 : ill <https://ieeexplore.ieee.org/document/793132>

Exploring the real-world challenges and efficacy of internal coupling in metastructures : an experimental perspective

Alimohammadi, Hossein; Vassiljeva, Kristina; Hosseinnia, S. Hassan; Ellervee, Peeter; Petlenkov, Eduard 2024 International Conference on Electrical, Computer and Energy Technologies (ICECET) 2024 <https://doi.org/10.1109/ICECET61485.2024.10698725> [Article at Scopus](#)

Fast fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings of East-West Design & Test Workshop (EWDWTW'04) : Yalta, Alushta, Crimea, Ukraine, September 23-26, 2004 2004 / p. 35-40 <https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=a6eb712498a5f23db3f95ad66bada257c21e96f0>

Fast RTL fault simulation using decision diagrams and bitwise set operations

Reinsalu, Uljana; Raik, Jaan; Ubar, Raimund-Johannes; Ellervee, Peeter 2011 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) : 3-5 October 2011, Vancouver, Canada 2011 / p. 164-170 <https://ieeexplore.ieee.org/document/6104440>

Fault emulation on FPGA : a feasibility study

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin IEEE NORCHIP 2003 : 21 Norchip Conference : Riga, Latvia, 10-11 November 2003 : proceedings 2003 / p. 92-95 : ill https://www.researchgate.net/publication/246171898_Fault_Emulation_on_FPGA_A_Feasibility_Study

Fault simulation and code coverage analysis of RTL designs using high-level decision diagrams = Rikete simuleerimine ja koodikatte analüüs register-siirde tasemel kasutades kõrgtaseme otsustusdiagramme

Reinsalu, Uljana 2013 https://www.ester.ee/record=b2963595*est

Fault simulation of digital systems = Digitaalsüsteemide rikete simuleerimine

Devadze, Sergei 2009 <https://digi.lib.ttu.ee/ii/?445> https://www.ester.ee/record=b2508727*est

Flexible controller for educational robot kit

Ruberg, Priit; Guitar, Aivar; Ellervee, Peeter 2015 International Conference on Microelectronic Systems Education : MSE '15 : Pittsburgh, PA, May 20-21, 2015 2015 / p. 17-20 : ill <http://dx.doi.org/10.1109/MSE.2015.7160007>

Foreword : [selected papers of the 19th Biennial Conference on Electronics and Embedded Systems 2024 (BEC 2024), that took place on October 2-4, 2024, in Tallinn, Estonia]

Le Moullec, Yannick; Ellervee, Peeter Proceedings of the Estonian Academy of Sciences 2025 / p. 267-268
<https://doi.org/10.3176/proc.2025.2S.04>

Four years of System-on-Chip curricula

Kruus, Margus; Ellervee, Peeter EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 88-91

FPGA based emulation environment

Jervan, Gert; Arhipov, Anton; Ellervee, Peeter 2nd International Workshop on Reconfigurable Communication Centric System-on-Chip (ReCoSoC'06) 2006

FPGA based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tihomirov, Valentin; **Ubar, Raimund-Johannes** Proceedings [of] 22nd NORCHIP Conference : Oslo, Norway, 8-9 November 2004 2004 / p. 59-62 <https://ieeexplore.ieee.org/abstract/document/1423822>

FPGA based system for video compression and transmission over bluetooth

Gorev, Maksim; Ellervee, Peeter 53rd IEEE International Midwest Symposium on Circuits and Systems : Seattle, Washington, USA, August 1-4, 2010 : proceedings 2010 / p. 367-370 : ill <https://ieeexplore.ieee.org/document/5548853>

FPGA-based fault emulation of synchronous sequential circuits

Ellervee, Peeter; Raik, Jaan; Tammemäe, Kalle; **Ubar, Raimund-Johannes** IET computers and digital techniques 2007 / 2, p. 70-76 : ill <https://ieeexplore.ieee.org/abstract/document/1423822>

FPGA-based implementation of EEG analyzer

Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Jenihhin, Maksim; Ellervee, Peeter DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p
<https://www.microsoft.com/en-us/research/wp-content/uploads/2017/03/ellervee.pdf>

Functional self-test of high-performance pipe-lined signal processing architectures

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter; Devadze, Sergei; Raik, Jaan; Min, Mart Microprocessors and microsystems 2015 / p. 909-918 : ill <https://doi.org/10.1016/j.micpro.2014.11.002> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Generalization of network-on-chip communication modelling

Ellervee, Peeter; Tagel, Mihkel; Jervan, Gert Workshop Digest. Diagnostic Services in Network-on-Chips - Test, Debug, and On-Line Monitoring : DATE 2009 : Nice, France, 20-24 April, 2009 2009 / ? p

A generic scheme for communication representation and mapping

Meinke, Thomas; Jantsch, Axel; **Ellervee, Peeter;** Hemani, Ahmed; Tenhunen, Hannu 17th NORCHIP Conference : Oslo, Norway, 8-9 November 1999 : proceedings 1999 / p. 334-339 : ill
https://www.researchgate.net/publication/2598862_A_Generic_Scheme_for_Communication_Representation_and_Mapping

Guest editorial

Ellervee, Peeter; Nurmi, Jari Microprocessors and microsystems 2013 / p. 430-431

Guest editorial : implementation issues in system-on-chip

Ellervee, Peeter; Nurmi, Jari Journal of signal processing systems 2017 / p. 269-270 <https://doi.org/10.1007/s11265-017-1242-x> [Journal metrics at Scopus](#) [Article at Scopus](#) [Journal metrics at WOS](#) [Article at WOS](#)

Hardware close programming for freshmen

Kruus, Helena; Brik, Marina; Kruus, Margus; Ruberg, Priit; Viies, Vladimir; Ellervee, Peeter 10th European Workshop on Microelectronics Education : EWME 2014 : May 14-16, 2014, Tallinn, Estonia 2014 / p. 93-96 : ill

Hardware implementation of face recognition using low precision representation

Dwivedi, Sai Kumar; Azad, Siavoosh Payandeh; Ellervee, Peeter; Dash, Ratnakar BEC 2016 : 2016 15th Biennial Baltic Electronics Conference : proceedings of the 15th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 3-5, 2016, Tallinn, Estonia 2016 / p. 63-66 : ill http://www.ester.ee/record=b2150914*est

Hardware/Software co-design in practice : MEMOCODE'08 contest experience

Reinsalu, Uljana; Devadze, Sergei; Jutman, Artur; Tšertov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 55-58 : ill

HDL-s for students with different background

Reinsalu, Uljana; Arhipov, Anton; Evartson, Teet; Ellervee, Peeter Proceedings MSE 2007 : 2007 IEEE International Conference on Microelectronic Systems Education : 3-4 June 2007, San Diego, CA 2007 / p. 69-70
<https://ieeexplore.ieee.org/document/4231454>

Hierarchical calculation of malicious faults for evaluating the fault-tolerance

Ubar, Raimund-Johannes; Devadze, Sergei; Jenihhin, Maksim; Raik, Jaan; Jervan, Gert; Ellervee, Peeter Proceedings : Fourth IEEE International Symposium on Electronic Design, Test and Applications : [DELTA 2008] : 23-25 January 2008, Hong Kong, SAR, China 2008 / p. 222-227 : ill <https://ieeexplore.ieee.org/document/4459544>

High speed data preprocessing for bioimpedance measurements : architectural exploration

Ellervee, Peeter; Annus, Paul; Min, Mart The 27th NORCHIP Conference : Trondheim, Norway, November 2009 2009 / [4] p
<https://ieeexplore.ieee.org/document/5397838>

High-Level Decision Diagram manipulations for code coverage analysis

Minakova, Karina; Reinsalu, Uljana; Tšepurov, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter BEC 2008 : 2008 International Biennial Baltic Electronics Conference : proceedings of the 11th Biennial Baltic Electronics Conference : Tallinn University of Technology : October 6-8, 2008, Tallinn, Estonia 2008 / p. 207-210 : ill

High-level synthesis of control and memory intensive applications : thesis submitted to the Royal Institute of Technology in partial fulfillment of the requirements for the degree of Doctor of Technology

Ellervee, Peeter 2000

High-level synthesis of control and memory intensive communication systems

Ellervee, Peeter Eighth Annual IEEE International ASIC Conference and Exhibit : proceedings : Stouffer Renaissance Austin Hotel, Austin, Texas, September 18-22, 1995 1995 / p. 185-191 : ill

How to emulate Network-on-Chip?

Ellervee, Peeter; Jervan, Gert Proceedings of the IEEE East-West Design & Test Workshop (EWDWTW'06) : Sochi, Russia, September 15-19, 2006 2006 / p. 282-286 : ill

A HW/SW partitioning technique based on hierarchical canitate selection scheme

Jantsch, Axel; Ellervee, Peeter; Öberg, Johnny; Hemani, Ahmed 7th International Workshop on High-level Synthesis, Niagara-on-the Lake, Ontario, Canada, May 18-20, 1994 1994

IEEE Norchip 2003. a. konverents

Ellervee, Peeter A & A 2004 / 1, lk. 48-49 https://artiklid.elnet.ee/record=b1015000*est

Implementation of multisine signal generator for a bioimpedance measurement device

Gorev, Maksim; Pesonen, Vadim; Ellervee, Peeter BEC 2012 : 2012 13th Biennial Baltic Electronics Conference : proceedings of the 13th Biennial Baltic Electronics Conference : October 3-5, 2012, Tallinn, Estonia 2012 / p. 275-278 : ill

Improved fault emulation for synchronous sequential circuits

Raik, Jaan; Ellervee, Peeter; Tihomirov, Valentin; Ubar, Raimund-Johannes Proceedings : DSD'2005 : 8th Euromicro Conference on Digital System Design : Architectures, Methods and Tools : Porto, Portugal, August 30 - September 3, 2005 2005 / p. 72-78 : ill

Improved VHDL input for high-level synthesis tool xTractor

Ellervee, Peeter; Ivask, Eero; Kruus, Margus BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 87-90 : ill

Innovation and entrepreneurship in the computer systems curricula and Nordic Master School in innovative ICT

Jervan, Gert; Ellervee, Peeter; Kruus, Margus 22nd EAAEE annual conference : June, 13-15, 2011, Maribor, Slovenija : conference book 2011 / p. 9 <https://ieeexplore.ieee.org/document/6165723>

Introducing computer systems related topics in the first study semester

Gorev, Maksim; Pesonen, Vadim; Ellervee, Peeter Proceedings of the 8th European Workshop on Microelectronics Education : EWME 2010 : Darmstadt, Germany, 10-12 May 2010 / p. 185-188 : ill
https://www.researchgate.net/publication/228980104_Introducing_Computer_Systems_Related_Topics_in_the_First_Study_Semester

Involving students in teaching process — encouraging student-generated content in ICT studies

Kruus, Helena; Ellervee, Peeter; Robal, Tarmo; Ruberg, Priit; Kruus, Margus Proceedings of the 24th International Conference on European Association for Education in Electrical and Information Engineering : 30-31 May 2013, Chania, Greece 2013 / p. 76-81 : ill

IRSYD : an internal representation for heterogeneous embedded systems

Ellervee, Peeter Proceedings of NORCHIP'98 Conference, November 9-10, 1998, Lund, Sweden 1998 / p. 214-221 : ill

Journal of signal processing systems for signal, image, and video technology. Implementation issues in system-on-chip

2017 <https://link.springer.com/journal/11265/87/3/page/1>

JÄNES : a NAS framework for ML-based EDA applications

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems 2021 <https://doi.org/10.1109/DFT52944.2021.9568321>

Kaks uut unikaalset TalTechi magistrikava hakkavad valmistama ette tippspetsialiste strateegiliselt tähtsale IKT valdkonnale

digi.geenius.ee 2023 [Kaks uut unikaalset TalTechi magistrikava hakkavad valmistama ette tippspetsialiste strateegiliselt tähtsale IKT valdkonnale](#)

Kas sind huvitab, mis toimub “kapoti all”? TalTechi magistriõpe avab tehnoloogia telgitagused

digi.geenius.ee 2025 <https://digi.geenius.ee/blogi/teadus-ja-tulevik/kas-sind-huvitab-mis-toimub-kapoti-all-taltech-magistriope-avab-tehnoloogia-telgitagused/>

Keerukate arvutisüsteemide uurimine Tallinna Tehnikaülikoolis

Jervan, Gert; Ellervee, Peeter; Ubar, Raimund-Johannes Tallinna Tehnikaülikooli aastaraamat 2007 2008 / lk. 42-60 : ill

Kiibiargonaudid, nende kuldvillak ja sümplegaadid

Tammemäe, Kalle; Ellervee, Peeter Informaatika perspektiivsed suunad : Eesti Teaduste Akadeemia seminari materjalid : 29.11.2000 2000 / lk. 17-20 : ill

Kuidas mõjutab kiipsüsteem elektroonika-alast kõrgharidust?

Ellervee, Peeter A & A 2002 / 1, lk. 50-52

Mapping of VHDL structures for generic EDA database format IRSYD

Ivask, Eero; Ellervee, Peeter The 7th Biennial Conference on Electronics and Microsystem Technology "Baltic Electronics Conference" : BEC 2000 : October 8 - 11, 2000, Tallinn, Estonia : conference proceedings 2000 / p. 317-320 : ill

Microcontroller energy consumption estimation based on software analysis for embedded systems

Ruberg, Priit; Lass, Keijo; Ellervee, Peeter 2015 Nordic Circuits and Systems Conference (NORCAS) : NORCHIP & International Symposium on System-on-Chip (SoC) : 1st IEEE NORCAS Conference : 26-28 October 2015, Oslo, Norway 2015 / [4] p. : ill
<http://dx.doi.org/10.1109/NORCHIP.2015.7364397>

Microprocessors and microsystems : MICPRO : embedded hardware design

2010

ML-based online design error localization for RISC-V implementations

Selg, Hardi; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2023 IEEE 29th International Symposium on On-Line Testing and Robust System Design (IOLTS) : IOLTS 2023 : July 3rd-5th, 2023, Plataniás, Chania (Crete), Greece : proceedings 2023 / 7 p.
<https://doi.org/10.1109/IOLTS59296.2023.10224864>

Morphable compression architecture for efficient configuration in CGRAs

Jafri, Syed Mohammad Asad Hassan; Tajammul, Muhammad Adeel; Ellervee, Peeter 2014 17th Euromicro Conference on Digital System Design : DSD 2014 : 27-29 August 2014, Verona, Italy : proceedings 2014 / p. 42-49 : ill

Multisine and binary multifrequency waveforms in impedance spectrum measurement : a comparative study

Annus, Paul; Min, Mart; Ojarand, Jaan; Paavle, Toivo; Land, Raul; Ellervee, Peeter; Parve, Toomas 5th European Conference of the International Federation for Medical and Biological Engineering : 14-18 September 2011, Budapest, Hungary 2012 / p. 1265-

Multisine signal generation method for a bioimpedance measurement device

Gorev, Maksim; Pesonen, Vadim; Ellervee, Peeter Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 111-114 : ill

NESTIMATOR - a neural network based estimator

Ellervee, Peeter; Jantsch, Axel; Öberg, Johnny; Hemani, Ahmed 7th International Workshop on High-Level Synthesis, Niagara-on-the-Lake, Ontario, Canada, May 18-20, 1994 1994

NESTIMATOR - a neural network based estimator

Ellervee, Peeter 2nd Baltic Summer School on Information Technology and Systems Engineering, 25-28 July 1994, Nelijärve 1994

Neural network based estimator to explore the design space at system level

Ellervee, Peeter; Öberg, Johnny; Jantsch, Axel; Hemani, Ahmed BEC : Baltic Electronics Conference : proceedings of the 4th Biennial Conference, October 9-14, 1994, Tallinn (Estonia). 2 1994 / p. 391-396: ill https://www.eester.ee/record=b2150914*est

Open source on-chip logic analyzer for FPGA-s

Ehrenpreis, Lauri; Ellervee, Peeter; Tammemäe, Kalle BEC 2006 : 2006 International Baltic Electronics Conference : Tallinn University of Technology, October 2-4, 2006, Tallinn, Estonia : proceedings of the 10th Biennial Baltic Electronics Conference 2006 / p. 99-102 : ill

Optimization of multisine excitation for a bioimpedance measurement device

Ojarand, Jaan; Annus, Paul; Min, Mart; Gorev, Maksim; Ellervee, Peeter I2MTC 2014 IEEE International Instrumentation and Measurement Technology Conference : Instrumentation and Measurement for Sustainable Development : Radisson Montevideo Victoria Plaza Hotel & Conference Center, May 12-15, 2014, Montevideo, Uruguay : proceedings 2014 / p. 829-832 : ill <https://doi.org/10.1109/I2MTC.2014.6860859> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Performance estimation of embedded applications on microcontrollers

Ruberg, Priit; Lass, Keijo; Liiv, Elvar; Ellervee, Peeter 2017 IEEE Nordic Circuits and Systems Conference (NORCAS 2017): NORCHIP and International Symposium of System-on-Chip (SoC 2017) : Linköping, Sweden, 23-25 October, 2017 2017 / p. 170-175 : ill <http://dx.doi.org/10.1109/NORCHIP.2017.8124964>

Piezoelectric compensation of structural damping in metamaterial beams: stability and performance analysis

Alimohammadi, Hossein; Vassiljeva, Kristina; HosseinNia, S. Hassan; **Ellervee, Peeter; Petlenkov, Eduard** Active and Passive Smart Structures and Integrated Systems XVIII 2024 / art. 129460J, 11 p. : ill <https://doi.org/10.1117/12.3024120> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Polymorphic configuration architecture for CGRAs

Jafri, Syed Mohammad Asad Hassan; **Tajammul, Muhammad Adeel**; Hermani, Ahmed; Paul, Kolin; Plosila, Juha; **Ellervee, Peeter**; Tenhunen, Hannu IEEE transactions on Very Large Scale Integration (VLSI) Systems 2016 / p. 403-407 : ill <http://dx.doi.org/10.1109/TVLSI.2015.2402392>

Polynomial curve fitting by substitution

Gorev, Maksim; Pesonen, Vadim; Ellervee, Peeter FPGAWorld'11 : the 8th Annual FPGAWorld Conference : Copenhagen, Stockholm, Munich, September 12-15, 2011 2011 / [4] p.: ill <https://dl.acm.org/doi/pdf/10.1145/2157871.2157872>

Power-performance trade-offs in second level memory used by an ARM-like Risc architecture

Puttaswamy, Kiran; **Ellervee, Peeter** Power aware computing 2002 / ? p. [chapter 11] https://link.springer.com/chapter/10.1007/978-1-4757-6217-4_11

Reconfigurable data acquisition unit for bioimpedance measurements

Pesonen, Vadim; Gorev, Maksim; Annus, Paul; Min, Mart; Ellervee, Peeter BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 257-260 : ill

Reprogrammable data acquisition unit to reduce aliasing effect in bioimpedance measurements

Pesonen, Vadim; Gorev, Maksim; Annus, Paul; Min, Mart; Ellervee, Peeter The 7th Annual FPGA World Conference, Copenhagen, Denmark, 6 September 2010 2010 / [6] p.: ill https://www.researchgate.net/publication/238346996_Reprogrammable_data_acquisition_unit_to_reduce_aliasing_effect_in_bioimpedance_measurements

Research in digital design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Jervan, Gert; Jutman, Artur; Raik, Jaan; Ellervee, Peeter; Kruus, Margus Radioelectronics & informatics 2008 / p. 4-12 : ill <http://www.ewdtest.com/ri/%E2%84%96-1-40-january-march-2008/>

Research on digital system design and test at Tallinn University of Technology

Ubar, Raimund-Johannes; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert; Jütman, Artur; Kruus, Margus; Raik, Jaan
Research in Estonia : present and future 2011 / p. 184-205 : ill

Revolver : a high-performance MIMD architecture for collision free computing

Öberg, I.; **Ellervee, Peeter** Euromicro Conference : proceedings : 24th Euromicro Conference : Västerås, Sweden, August 25-27, 1998. Vol. 1 1998 / p. 301-308 <https://ieeexplore.ieee.org/document/711814>

Riistvara kirjelduskeel Verilog

Ellervee, Peeter A & A 1998 / 1, lk. 6-10

SCAAT: Secure cache alternative address table for mitigating cache logical side-channel attacks

Shalabi, Ameer; Ghasempouri, Tara; Ellervee, Peeter; Raik, Jaan 2020 23rd Euromicro Conference on Digital System Design (DSD), 26-28 August 2020, Kranj, Slovenia 2020 / art, 20035366, p. 213-217 <https://doi.org/10.1109/DSD51259.2020.00043>

Scheduling framework for dependable NoC-based systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Workshop Digest. Diagnostic Services in Network-on-Chips - Test, Debug, and On-Line Monitoring : DATE 2009 : Nice, France, 20-24 April, 2009 2009 / ? p <https://ieeexplore.ieee.org/document/5335670>

Scheduling framework for real-time dependable NoC-based systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Proceedings of the 11th International Conference on System-on-chip : Tampere, Finland, October 05-07, 2009 2009 / p. 95-99 <https://ieeexplore.ieee.org/document/5335670/keywords#keywords>

Self-testing of pipe-lined signal processing architectures at-speed

Gorev, Maksim; Ubar, Raimund-Johannes; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK seitsmenda aastakonverentsi artiklite kogumik : 15.-16. novembril 2013, Haapsalu 2013 / p. 25-28 : ill

SoC curricula at Tallinn Technical University

Kruus, Margus; Tammemäe, Kalle; Ellervee, Peeter 19th NORCHIP Conference, Kista, Sweden, 12-13 November 2001 : proceedings 2001 / p. 99-104 : ill

SoCDep2 : a framework for dependable task deployment on many-core systems under mixed-criticality constraints

Azad, Siavoosh Payandeh; Niazmand, Behrad; Ellervee, Peeter; Raik, Jaan; Jervan, Gert; Hollstein, Thomas 2016 11th International Symposium on Reconfigurable Communication-centric Systems-on-Chip (ReCoSoC) : June 27-29, 2016, Tallinn, Estonia 2016 / [6] p. : ill <https://doi.org/10.1109/ReCoSoC.2016.7533903>

Software parser and analyser for hardware performance estimations

Ruberg, Priit; Meinberg, Erki; Ellervee, Peeter 2022 International Conference on Electrical, Computer and Energy Technologies (ICECET), Prague, Czech Republic, 20-22 July 2022 2022 / p. 1-6 <https://doi.org/10.1109/ICECET55527.2022.9872951>

Special session: in-field ML-assisted intermittent fault localization and management in RISC-V SoCs

Selg, Hardi; Shibin, Konstantin; Tsertov, Anton; Jenihhin, Maksim; Ellervee, Peeter; Raik, Jaan 2024 IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT) 2024
<https://doi.org/10.1109/DFT63277.2024.10753541> [Conference proceedings at Scopus](#) [Article at Scopus](#) [Article at WOS](#)

Standards-based tools and services for building lifelong learning pathways

Sgouroupoulou, C.; Voyiatzis, I.; Koutoumanos, A.; **Ellervee, Peeter** Proceedings of 2017 IEEE Global Engineering Education Conference (EDUCON) : 25-28 April 2017, Athens, Greece 2017 / p. 1619-1621 <https://doi.org/10.1109/EDUCON.2017.7943065>
<https://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=7943065>

Surviving the unforeseen - teaching IT and engineering students during COVID-19 outbreak

Ruberg, Priit; Ellervee, Peeter; Tammemäe, Kalle; Reinsalu, Uljana; Rähni, Andres; Robal, Tarmo Proceedings - Frontiers in Education Conference, FIE 2022 / Code 184790 <https://doi.org/10.1109/FIE56618.2022.9962383> [Conference Proceedings at Scopus](#)
[Article at Scopus](#)

System level power-performance trade-offs in embedded systems using voltage and frequency scaling of off-chip buses and memory

Puttaswamy, Kiran; Choi, Kyu-Won; Park, Jun Cheol; Mooney III, Vincent J.; Chatterjee, Abhijit; **Ellervee, Peeter** ISSS'02, October 2-4, 2002, Kyoto, Japan 2002 / p. 225-230 : ill <https://ieeexplore.ieee.org/document/1227182>

System-level communication synthesis and dependability improvements for Network-on-Chip based systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Estonian journal of engineering 2010 / 1, p. 23-38 : ill
https://artiklid.elnet.ee/record=b1964968*est

System-level data format exploration for dynamically allocated data structures

Ellervee, Peeter; Miranda, Miguel; Cathoor, Francky; Hemani, Ahmed IEEE transactions on computer-aided design of integrated circuits and systems 2001 / 12, p. 1469-1472 : ill <https://ieeexplore.ieee.org/abstract/document/969440>

System-level data format exploration for dynamically allocated data structures

Ellervee, Peeter; Miranda, Miguel; Cathoor, Francky; Hemani, Ahmed 37th Design Automation Conference : Los Angeles, CA, June 5-9, 2000 : proceedings 2000 / p. 556-559 : ill <https://ieeexplore.ieee.org/document/855373>

System-level design of NoC-based dependable embedded systems

Tagel, Mihkel; Ellervee, Peeter; Jervan, Gert Design and test technology for dependable systems-on-chip 2011 / p. 1-36 : ill https://pld.ttu.ee/~raiub/BOOK_content/Section_1/Ch11_jervan/Ch11_jervan_.pdf

System-level optimization of NoC-based timing sensitive systems

Tagel, Mihkel; Ellervee, Peeter; Hollstein, Thomas; Jervan, Gert Estonian journal of engineering 2011 / 2, p. 158-168 : ill https://artiklid.elnet.ee/record=b2422982*est

Teaching HDL for IT-students

Ellervee, Peeter; Reinsalu, Uljana; Arhipov, Anton EWME 2006 proceedings : 6th International Workshop on Microelectronics Education : 8-9 June, 2006, Stockholm, Sweden 2006 / p. 112-115

Tehismehikesed rallisid miinirajal : [21. nov. TTÜ aulas toimunud robotite võistlusest Robotex 2003 : TTÜ võistkonnad said 2. ja 3. koha : kommenteerib Peeter Ellervee]

Ellervee, Peeter; Kaupmees, Greta SL Õhtuleht 2003 / 24. nov., lk. 28 : ill

TOP : an algorithm for three-level optimization of PLDs

Dubrova, E.; **Ellervee, Peeter**; Miller, D.M.; Muzio, J.C. Design, Automation and Test in Europe : Conference and Exhibition 2000 : Paris, France, March 27-30, 2000 : proceedings 2000 / p. 751

Translating behavioral VHDL for emulation

Ellervee, Peeter; Reinsalu, Uljana; Arhipov, Anton 25th IEEE NORCHIP Conference : Aalborg, Denmark, 19-20 November 2007 2007 / ? p <https://ieeexplore.ieee.org/document/4481073>

TransMem : a memory architecture to support dynamic remapping and parallelism in low power high performance CGRAs

Tajammul, Muhammad Adeel; Jafri, Syed Mohammad Asad Hassan; Hemani, Ahmed; **Ellervee, Peeter** 2016 26th International Workshop on Power and Timing Modeling, Optimization and Simulation : PATMOS 2016 : September, 21st to 23th 2016, Bremen, Germany : proceedings 2016 / p. 92-99 : ill <https://doi.org/10.1109/PATMOS.2016.7833431>

2018 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC) : 30-31 October 2018, Tallinn, Estonia : proceedings in IEEE Xplore [Online resource]

2018 <https://ieeexplore.ieee.org/xpl/conhome/8552599/proceeding>

2019 IEEE Nordic Circuits and Systems Conference (NORCAS) : NORCHIP and International Symposium of System-on-Chip (SoC), 29-30 October 2019, Helsinki, Finland : proceedings in IEEE Xplore 2019

2023 IEEE Nordic Circuits and Systems Conference (NORCAS) : 31 October-November 1, 2023 Aalborg, Denmark : proceedings in IEEE Xplore

2023 <https://researchr.org/publication/norcas-2023>

Using emulation for system model analysis

Ellervee, Peeter; Arhipov, Anton; Reinsalu, Uljana DATE'07 Friday Workshop on "Diagnostic Service in Network-on-Chips" : Nice, France, 16-20 April 2007 2007 / p. 280-282

Using soft-core processors and FPGA development boards for hardware emulation

Arhipov, Anton; Ellervee, Peeter Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 155-158 : ill

Using weighted graph coloring heuristics for architecture exploration

Ellervee, Peeter; Klaar, Tarmo 19th NORCHIP Conference, Kista, Sweden, 12-13 November 2001 : proceedings 2001 / p. 161-166 : ill

Using weighted graphs for fast architecture exploration

Ellervee, Peeter; Klaar, Tarmo; **Kruus, Margus; Tammemäe, Kalle** BEC 2002 : proceedings of the 8th Biennial Baltic Electronics Conference : October 6-9, 2002, Tallinn, Estonia 2002 / p. 111-114 : ill

Wafer-level die re-test success prediction using machine learning

Selg, Hardi; **Jenihhin, Maksim; Ellervee, Peeter** 21st IEEE Latin-American Test Symposium (LATS) 2020 : proceedings 2020 / 5 p <https://doi.org/10.1109/LATS49555.2020.9093672>

Variable byte-length data compression algorithm

Gorev, Maksim; Ellervee, Peeter BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 353-356 : ill

VHDL front-end for high-level synthesis tool xTractor

Ivask, Eero; Ellervee, Peeter BEC 2004 : proceedings of the 9th Biennial Baltic Electronics Conference : October 3-6, 2004, Tallinn, Estonia 2004 / p. 111-114 : ill

XT taskus : [taskuarvutitest]

Ellervee, Peeter Arvutustehnika ja Andmetöötlus 1990 / 12, lk. 1-2

xTractor : an academic high-level synthesis tool for control and memory intensive applications

Ellervee, Peeter University Booth at Design and Test in Europe : DATE'05 : Munich, Germany, 2005 2005 / ? p
<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=6db1d71884b75b47fb27ae86b91b61894e57fd18>

xTractor: an academic higg-level synthesis tool for control and memory intensive applications

Ellervee, Peeter 20th IEEE Conference NORCHIP'2002, Copenhagen, Denmark 2002 / p. 253-258
<https://citeseerx.ist.psu.edu/document?repid=rep1&type=pdf&doi=6db1d71884b75b47fb27ae86b91b61894e57fd18>

Оптимизация базиса сети при декомпозиции микропрограммных автоматов

Leis, Paul; Ellervee, Peeter Методы синтеза и диагностирования цифровых схем 1985 / с. 19-25

Построение контрольной последовательности для управляющих автоматов, реализованных на программируемых логических матриц

Kaširova, Lilia; Kruus, Margus; Ellervee, Peeter Машинное проектирование электронных устройств и систем 1989 / с. 77-88

Электротехника и автоматика

Pikkov, Otto; Keevallik, Andres; Lausmaa, Toomas; Sudnitsõn, Aleksander; Leis, Paul; Ellervee, Peeter; Berkman, Boriss; Alango, Villem; Kitsnik, Peeter; Kont, Toomas; Kruus, Margus; Ubar, Raimund-Johannes; Evertson, Teet; Lohuaru, Tõnu; Räisa, O.; Toome, Tõnis; Šendrik, M.G.; Tamm, Boris, inform. 1985 https://www.ester.ee/record=b1356648*est

Электротехника и автоматика

Mägi, Harri; Velmre, Enn; Pikkov, Mihhail; Orro, S.; Rang, Toomas; Gurjanov, Boris; Kruus, Margus; Salum, Kaja; Berkman, Boriss; Keevallik, Andres; Kaširova, Lilia; Kruus, Margus; Ellervee, Peeter; Ubar, Raimund-Johannes; Grigorjeva, Ksenja; Kont, Toomas 1989 https://www.ester.ee/record=b1285446*est