

Abstraction of clock interface for conversion of RTL VHDL to SystemC

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Conversion error of exponential to second order polynomial ZIP load model conversion

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High-performance analogue measurement using internal enhanced PWM and ADC of a DSP-chip

Märtens, Olev; Min, Mart; Trampärk, Harri; Liimets, Aivar WISP2007 proceedings : 5th IEEE International Symposium on Intelligent Signal Processing : Alcala de Henares, Madrid (Spain), October 3-5, 2007 2007 / [5] p <https://ieeexplore.ieee.org/document/4447593>

Влияние неидеальностей кос на качество преобразования импеданса

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