

Acceleration of recursive data sorting over tree-based structures

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Sklyarov, Valery; Skliarova, Iuliia Elektronika ir elektrotehnika = Electronics and electrical engineering 2011 / p. 51-56 : ill <https://eejournal.ktu.lt/index.php/elt/article/view/612>

Address-based data processing over N-ary trees

Sklyarov, Valery; Skliarova, Iuliia; **Kruus, Margus; Mihhailov, Dmitri; Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

Advanced topics of FSM design using FPGA educational boards and web-based tools

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 446-449 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5742086>

Application-specific hardware accelerator for implementing recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Proceedings of the IEEE International Conference on Field Programmable Technology (FPT'10) : Beijing, China Dec. 8-10, 2010 2010 / p. 269-272 : ill <https://ieeexplore.ieee.org/document/5681486>

Architectural solutions for high-speed data processing demands of CERN LHC detectors with FPGA and high-level synthesis

Devadze, Sergei; Nielsen, Christine Elizabeth; **Mihhailov, Dmitri; Ellervee, Peeter** 2024 IEEE Nordic Circuits and Systems Conference (NorCAS) 2024 <https://doi.org/10.1109/NorCAS64408.2024.10752490> [Article at Scopus](#)

Cooperation of FPGA-based educational boards and web-based point design tools for research and education

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus IFIP EduTech'09 International Workshop : Florianopolis-Brazil, October 15-16, 2009 2009 / ? p

EEG analyzer prototype based on FPGA

Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Ellervee, Peeter; Hinrikus, Hiie; Bachmann, Maie; Lass, Jaanus 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011) : September 4-6, 2011, Dubrovnik, Croatia : proceedings 2011 / p. 101-106 : ill <https://ieeexplore.ieee.org/document/6046588>

FPGA platform based digital design education

Mihhailov, Dmitri; Kruus, Margus; Sudnitsõn, Aleksander Proceedings of the 9th International Conference on Computer Systems and Technologies and Workshop for PhD Students in Computing : CompSysTech'2008. Vol. 374, ACM International Conference Proceeding Series 2008 / p. IV.4-1 - IV.4-6 : ill <https://dl.acm.org/doi/pdf/10.1145/1500879.1500938>

FPGA-based implementation of EEG analyzer

Gorev, Maksim; Pesonen, Vadim; Mihhailov, Dmitri; Jenihhin, Maksim; Ellervee, Peeter DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p <https://www.microsoft.com/en-us/research/wp-content/uploads/2017/03/ellervee.pdf>

FPGA-based implementation of EEG analyzer for detection of depressive disorder

Pesonen, Vadim; Gorev, Maksim; Mihhailov, Dmitri Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 67-70 : ill

FSM decomposition with application to FPGA synthesis

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Kruus, Margus; Tarletski, Konstantin International Conference on Computer Systems and Technologies - CompSysTech'09 : Ruse, Bulgaria 2009 / p. IV.4.1-IV.4.6 <https://dl.acm.org/doi/10.1145/1731740.1731820>

Hardware implementation of recursive algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 53rd IEEE International Midwest Symposium on Circuits and Systems : Seattle, Washington, USA, August 1-4, 2010 : proceedings 2010 / p. 225-228 <https://ieeexplore.ieee.org/document/5548674>

Hardware implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA) : Kuala Lumpur, Malaysia, April 25-27, 2011 : [proceedings] 2011 / p. 33-38 : ill <https://ieeexplore.ieee.org/document/5959040>

Hardware implementation of recursive sorting algorithms using tree-like structures and HFSM models = Rekursiivsete sortimisalgoritmid riistvaraline realiseerimine kasutades puulaadseid struktuure ja HFSM mudeleid

Mihhailov, Dmitri 2011 https://www.ester.ee/record=b2748823*est

High-performance hardware accelerators for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 313-318 : ill

HLS-based optimization of tau triggering algorithm for LHC: a case study

Cherezova, Natalia; Mihhailov, Dmitri; Devadze, Sergei; Jutman, Artur 2022 18th Biennial Baltic Electronics Conference (BEC) 2022 / 6 p. : ill <https://doi.org/10.1109/BEC56180.2022.9935599>

Implementation in FPGA of address-based data sorting

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 21st International Conference on Field Programmable Logic and Applications : FPL 2011 : Chania, Crete, Greece, 5-7 September 2011 2011 / p. 405-410 : ill https://www.researchgate.net/publication/220760392_Implementation_in_FPGA_of_Address-Based_Data_Sorting

Implementation of address-based data sorting on different FPGA platforms

Sudnitsõn, Aleksander; Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia Proceedings of IEEE East-West Design & Test Symposium (EWDTS'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 38-41 <https://www.semanticscholar.org/paper/Implementation-of-address-based-data-sorting-on-Mihhailov-Sudnitsõn/e9294d725ab92a2d2a51ccb44fc47e80798bc071>

Implementation of sorting algorithms in reconfigurable hardware

Skliarova, Iuliia; Sklyarov, Valery; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2012 IEEE Mediterranean Electrotechnical Conference (MELECON 2012) : Yasmine Hammamet, Tunisia, March 25-28, 2012 2012 / p. 107-110 : ill <https://ieeexplore.ieee.org/document/6196391>

Multilevel models for data processing

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE GCC Conference and Exhibition (GCC) : February 19-22, 2011, Dubai, United Arab Emirates 2011 / p. 136-139

Optimization of address-based data sorting unit with external memory support

Mihhailov, Dmitri; Rjabov, Artjom; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** CompSysTech'13 : proceedings of the 14th International Conference on Computer Systems and Technologies 2013 / p. 83-90 : ill <https://doi.org/10.1145/2516775.2516807> [Conference Proceedings at Scopus](#) [Article at Scopus](#)

Optimization of FPGA-based circuits for recursive data sorting

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 129-132 : ill

Optimization of recursive sorting algorithms for implementation in hardware

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Proceedings of 22nd International Conference on Microelectronics (ICM 2010) : Cairo, Egypt, Dec. 19-22, 2010 2010 / p. 471-474 : ill https://www.researchgate.net/publication/224213497_Optimization_of_recursive_sorting_algorithms_for_implementation_in_hardware

Parallel FPGA-based implementation of recursive sorting algorithms

Mihhailov, Dmitri; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 121-126 : ill https://www.researchgate.net/publication/221437230_Parallel_FPGA-Based_Implementation_of_Recursive_Sorting_Algorithms

Performance evaluation for FPGA-based processing of tree-like structures

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 19th IEEE International Conference on Electronics, Circuits, and Systems (IEEE ICECS), Sevilla, Spain, December 9-12, 2012 2012 / p. 217-220 : ill <https://ieeexplore.ieee.org/document/6463762>

Processing N-ary trees in hardware circuits

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 13th International Symposium on Integrated Circuits (ISIC) : Singapore, 12-14 December 2011 : proceedings 2011 / p. 262-265 : ill <https://ieeexplore.ieee.org/document/6131946>

Processing tree-like data structures for sorting and managing priorities

Sklyarov, Valery; Skliarova, Iuliia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE Symposium on Computers & Informatics : ISC12011 : Kuala Lumpur, Malaysia, 20-23 March 2011 2011 / p. 322-327 https://www.researchgate.net/publication/252020117_Processing_tree-like_data_structures_for_sorting_and_managing_priorities

Processing tree-like data structures in different computing platforms

Sklyarov, Valery; Skliarova, Iuliia; Oliveira, Ramiro; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2011 International Conference on Information and Computer Applications (ICICA 2011) : Dubai, United Arab Emirates, March 18-20, 2011 2011 / p. 112-116 : ill https://sweet.ua.pt/iouliia/Papers/2011/rp025_ICICA2011-A067.pdf

Recursion and hierarchy in digital design and prototyping : a case study

Mihhailov, Dmitri; Kruus, Margus; Sklyarov, Valery; Skliarova, Iuliia; **Sudnitsõn, Aleksander** Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill

<https://dl.acm.org/doi/pdf/10.1145/2023607.2023616>

Synthesis and implementation of hierarchical finite state machines with implicit modules

Sklyarov, Valery; Skliarova, Ioulia; **Mihhailov, Dmitri; Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 436-441 : ill
https://www.researchgate.net/publication/221437255_Synthesis_and_Implementation_of_Hierarchical_Finite_State_Machines_with_Implicit_Modules

Web-based tool for FSM encoding targeting low-power FPGA implementation

Mihhailov, Dmitri; Sudnitsõn, Aleksander; Tarletski, Konstantin 2010 27th International Conference on Microelectronics : MIEL 2010 : Niš, Serbia, 16-19 May 2010 : proceedings 2010 / p. 349-352 <https://ieeexplore.ieee.org/document/5490468>