

Acceleration of recursive data sorting over tree-based structures

Mihailov, Dmitri; Sudnitsõn, Aleksander; Sklyarov, Valery; Sklarova, Ioulia Elektronika ir elektrotehnika = Electronics and electrical engineering 2011 / p. 51-56 : ill <https://eejournal.ktu.lt/index.php/elt/article/view/612>

Address-based data processing over N-ary trees

Sklyarov, Valery; Sklarova, Ioulia; **Kruus, Margus; Mihailov, Dmitri; Sudnitsõn, Aleksander** EuroCon 2013 : 01-04 July 2013, Zagreb, Croatia 2013 / p. 1790-1797 : ill

Advanced topics of FSM design using FPGA educational boards and web-based tools

Sudnitsõn, Aleksander; Mihailov, Dmitri; Kruus, Margus East-West Design & Test Symposium : Moscow, September 18-21, 2009 2009 / p. 446-449 <https://ieeexplore.ieee.org/stamp/stamp.jsp?arnumber=5742086>

Application-specific hardware accelerator for implementing recursive sorting algorithms

Mihailov, Dmitri; Sklyarov, Valery; Sklarova, Ioulia; Sudnitsõn, Aleksander Proceedings of the IEEE International Conference on Field Programmable Technology (FPT'10) : Beijing, China Dec. 8-10, 2010 2010 / p. 269-272 : ill

Cooperation of FPGA-based educational boards and web-based point design tools for research and education

Sudnitsõn, Aleksander; Mihailov, Dmitri; Kruus, Margus IFIP EduTech'09 International Workshop : Florianopolis-Brazil, October 15-16, 2009 2009 / ? p

EEG analyzer prototype based on FPGA

Jenihhin, Maksim; Gorev, Maksim; Pesonen, Vadim; Mihailov, Dmitri; Ellervee, Peeter; Hinrikus, Hii; Bachmann, Maie; Lass, Jaanus 7th International Symposium on Image and Signal Processing and Analysis (ISPA 2011) : September 4-6, 2011, Dubrovnik, Croatia : proceedings 2011 / p. 101-106 : ill

FPGA platform based digital design education

Mihailov, Dmitri; Kruus, Margus; Sudnitsõn, Aleksander Proceedings of the 9th International Conference on Computer Systems and Technologies and Workshop for PhD Students in Computing : CompSysTech'2008. Vol. 374, ACM International Conference Proceeding Series 2008 / p. IV.4-1 - IV.4-6 : ill

FPGA-based implementation of EEG analyzer

Gorev, Maksim; Pesonen, Vadim; Mihailov, Dmitri; Jenihhin, Maksim; Ellervee, Peeter DATE'11 Friday Workshop on "Design Methods and Tools for FPGA-Based Acceleration of Scientific Computing" : Grenoble, France, March 2011 2011 / [1] p

FPGA-based implementation of EEG analyzer for detection of depressive disorder

Pesonen, Vadim; Gorev, Maksim; Mihailov, Dmitri Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kuuenda aastakonverentsi artiklite kogumik : 3.-5. oktoobril 2012, Laulasmaa 2012 / p. 67-70 : ill

FSM decomposition with application to FPGA synthesis

Sudnitsõn, Aleksander; Mihailov, Dmitri; Kruus, Margus; Tarletski, Konstantin International Conference on Computer Systems and Technologies - CompSysTech'09 : Ruse, Bulgaria 2009 / p. IV.4.1-IV.4.6

Hardware implementation of recursive algorithms

Mihailov, Dmitri; Sklyarov, Valery; Sklarova, Ioulia; Sudnitsõn, Aleksander 53rd IEEE International Midwest Symposium on Circuits and Systems : Seattle, Washington, USA, August 1-4, 2010 : proceedings 2010 / p. 225-228

Hardware implementation of recursive sorting algorithms

Mihailov, Dmitri; Sklyarov, Valery; Sklarova, Ioulia; Sudnitsõn, Aleksander 2011 International Conference on Electronic Devices, Systems and Applications (ICEDSA) : Kuala Lumpur, Malaysia, April 25-27, 2011 : [proceedings] 2011 / p. 33-38 : ill

Hardware implementation of recursive sorting algorithms using tree-like structures and HFSM models = Rekursiivsete sortimisalgoritmide riistvaraline realiseerimine kasutades puulaadseid struktuure ja HFSM mudeleid

Mihailov, Dmitri 2011 https://www.esther.ee/record=b2748823*est

High-performance hardware accelerators for sorting and managing priorities

Sklyarov, Valery; Sklarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems : April 13-15, 2011, Gottbus, Germany 2011 / p. 313-318 : ill

HLS-based optimization of tau triggering algorithm for LHC: a case study

Cherezova, Natalia; Mihailov, Dmitri; Devadze, Sergei; Jutman, Artur 2022 18th Biennial Baltic Electronics Conference (BEC) 2022 / 6 p. : ill <https://doi.org/10.1109/BEC56180.2022.9935599>

Implementation in FPGA of address-based data sorting

Sklyarov, Valery; Sklarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 21st International Conference on Field Programmable Logic and Applications : FPL 2011 : Chania, Crete, Greece, 5-7 September 2011 2011 / p. 405-410 : ill

Implementation of address-based data sorting on different FPGA platforms

Sudnitsõn, Aleksander; Mihailov, Dmitri; Sklyarov, Valery; Skliarova, Ioulia Proceedings of IEEE East-West Design & Test Symposium (EWDTs'2012) : Kharkov, Ukraine, September 14–17, 2012 2012 / p. 38-41

Implementation of sorting algorithms in reconfigurable hardware

Sklyarov, Ioulia; Sklyarov, Valery; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 2012 IEEE Mediterranean Electrotechnical Conference (MELECON 2012) : Yasmine Hammamet, Tunisia, March 25-28, 2012 2012 / p. 107-110 : ill

Multilevel models for data processing

Sklyarov, Valery; Sklyarov, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE GCC Conference and Exhibition (GCC) : February 19-22, 2011, Dubai, United Arab Emirates 2011 / p. 136-139

Optimization of address-based data sorting unit with external memory support

Mihailov, Dmitri; Rjabov, Artjom; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** CompSysTech'13 : proceedings of the 14th International Conference on Computer Systems and Technologies 2013 / p. 83-90 : ill

Optimization of FPGA-based circuits for recursive data sorting

Mihailov, Dmitri; Sklyarov, Valery; Skliarova, Ioulia; Sudnitsõn, Aleksander BEC 2010 : 2010 12th Biennial Baltic Electronics Conference : proceedings of the 12th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 4-6, 2010, Tallinn, Estonia 2010 / p. 129-132 : ill

Optimization of recursive sorting algorithms for implementation in hardware

Mihailov, Dmitri; Sklyarov, Valery; Skliarova, Ioulia; Sudnitsõn, Aleksander Proceedings of 22nd International Conference on Microelectronics (ICM 2010) : Cairo, Egypt, Dec. 19-22, 2010 2010 / p. 471-474 : ill

Parallel FPGA-based implementation of recursive sorting algorithms

Mihailov, Dmitri; Sklyarov, Valery; Skliarova, Ioulia; Sudnitsõn, Aleksander 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 121-126 : ill

Performance evaluation for FPGA-based processing of tree-like structures

Sklyarov, Valery; Skliarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 19th IEEE International Conference on Electronics, Circuits, and Systems (IEEE ICECS), Sevilla, Spain, December 9-12, 2012 2012 / p. 217-220 : ill
<https://ieeexplore.ieee.org/document/6463762>

Processing N-ary trees in hardware circuits

Sklyarov, Valery; Skliarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 13th International Symposium on Integrated Circuits (ISIC) : Singapore, 12-14 December 2011 : proceedings 2011 / p. 262-265 : ill

Processing tree-like data structures for sorting and managing priorities

Sklyarov, Valery; Skliarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 2011 IEEE Symposium on Computers & Informatics : ISCI2011 : Kuala Lumpur, Malaysia, 20-23 March 2011 2011 / p. 322-327

Processing tree-like data structures in different computing platforms

Sklyarov, Valery; Skliarova, Ioulia; Oliveira, Ramiro; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 2011 International Conference on Information and Computer Applications (ICICA 2011) : Dubai, United Arab Emirates, March 18-20, 2011 2011 / p. 112-116 : ill

Recursion and hierarchy in digital design and prototyping : a case study

Mihailov, Dmitri; Kruus, Margus; Sklyarov, Valery; Skliarova, Ioulia; **Sudnitsõn, Aleksander** Computer Systems and Technologies : 12th International Conference, CompSysTech'11 : Vienna, Austria, June 16-17, 2011 : proceedings 2011 / p. 45-50 : ill

Synthesis and implementation of hierarchical finite state machines with implicit modules

Sklyarov, Valery; Skliarova, Ioulia; **Mihailov, Dmitri; Sudnitsõn, Aleksander** 2010 International Conference on Reconfigurable Computing and FPGAs (ReConFig 2010) : Cancun, Mexico, December 13-15, 2010 2010 / p. 436-441 : ill

Web-based tool for FSM encoding targeting low-power FPGA implementation

Mihailov, Dmitri; Sudnitsõn, Aleksander; Tarletski, Konstantin 2010 27th International Conference on Microelectronics : MIEL 2010 : Niš, Serbia, 16-19 May 2010 : proceedings 2010 / p. 349-352 <https://ieeexplore.ieee.org/document/5490468>