An external test approach for network-on-a-chip switches
Raik, Jaan; **Govind, Vineeth**; **Ubar, Raimund-Johannes** ATS '06 : Proceedings of the 15th Asian Test Symposium : November 20-23, 2006, Fukuoka, Japan 2006 / p. 437-442 : ill http://dx.doi.org/10.1109/ATS.2006.23

An external test approach for network-on-a-chip switches
Raik, Jaan; **Govind, Vineeth**; **Ubar, Raimund-Johannes** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 185-190 : ill

DfT for application of external test patterns in a Network-on-a-Chip
Govind, Vineeth; **Raik, Jaan**; **Ubar, Raimund-Johannes** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK kolmanda aastakonverentsi artiklite kogumik : 25.-26. aprill 2008, Voore külalistemaja 2008 / p. 25-28 : ill

DfT-based external test and diagnosis of mesh-like networks on chips = Testitavusel põhinev välise testi ja diagnoosi meetod kahemõõtmelistele kiipvõrkudele
Govind, Vineeth 2009 https://digi.lib.ttu.ee/i/?454 https://www.ester.ee/record=b2539211*est

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** Proceedings of the 8th Annual Conference of the Estonian National Doctoral School in Information and Communication Technologies : December 5-6, 2014, Rakvere 2014 / p. 83-86 : ill

Extended checkers for logic-based distributed routing in network-on-chips
Niazmand, Behrad; **Hariharan, Ranganathan**; **Govind, Vineeth**; **Jervan, Gert**; **Hollstein, Thomas**; **Raik, Jaan** BEC 2014 : 2014 14th Biennial Baltic Electronics Conference : proceedings of the 14th Biennial Baltic Electronics Conference : Tallinn University of Technology, October 6-8, 2014, Tallinn, Estonia 2014 / p. 77-80 : ill

A framework for combining concurrent checking and online embedded test for low-latency fault detection in NoC routers
Saltarelli, Pietro; **Niazmand, Behrad**; **Raik, Jaan**; **Govind, Vineeth**; **Hollstein, Thomas**; **Jervan, Gert**; **Hariharan, Ranganathan** NOCS '15 : International Symposium on Networks-on-Chip : Vancouver, BC, Canada, September 28-30, 2015 2015 / [8] p. : ill http://dx.doi.org/10.1145/2786572.2788713

Kuidas testida arvutivõrku ränikiibil
Raik, Jaan; **Govind, Vineeth** A & A 2010 / 4, lk. 35-37 https://artiklid.elnet.ee/record=b2286479*est

Low-area boundary BIST architecture for mesh-like network-on-chip
Raik, Jaan; **Govind, Vineeth** Proceedings of the 2012 IEEE 15th International Symposium on Design and Diagnostics of Electronic Circuits & Systems (DDECS) : April 18-20, 2012 Tallinn, Estonia 2012 / p. 95-100 : ill

Tenniseharrastus Tallinna tehnikaülikoolis. Tennis on au sees : [kommenteerivad Tauno Otto ja Viveeth Govind]
Sulling, Andres; **Otto, Tauno**; **Govind, Vineeth** Mente et Manu 2013 / lk. 26-27 : fot

Test configurations for diagnosing faulty links in NoC switches
Raik, Jaan; **Ubar, Raimund-Johannes**; **Govind, Vineeth** Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK teise aastakonverentsi artiklite kogumik : 11.-12. mai 2007, Viinistu kunstimuuseum 2007 / lk. 33-37 : ill

Test configurations for diagnosing faulty links in NoC switches
Raik, Jaan; **Ubar, Raimund-Johannes**; **Govind, Vineeth** 12th IEEE European Test Symposium ETS 2007 : 20-24 May 2007, Freiburg, Germany : proceedings 2007 / p. 29-34 : ill http://dx.doi.org/10.1109/ETS.2007.41

Ultra-low latency NoC testing via pseudo-random test pattern compaction
Tatenguem, Herve; **Govind, Vineeth**; **Raik, Jaan** SoC 2012 : International Symposium on System-on-Chip 2012 : Tampere, Finland, October 11-12, 2012 2012 / 6 p. : ill https://ieeexplore.ieee.org/document/6376370