

An approach for verification assertions reuse in RTL test pattern generation

Jenihhin, Maksim; Raik, Jaan; Fujiwara, Hideo; Ubar, Raimund-Johannes; Viilukas, Taavi Digest of papers : IEEE 11th Workshop on RTL and High Level Testing : WRTL'10 : December 5-6, 2010, Shanghai, China 2010 / p. 107-110 : ill

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Jenihhin, Maksim; Raik, Jaan; Ubar, Raimund-Johannes; Viilukas, Taavi; Fujiwara, Hideo Journal of Shanghai Normal University : Natural Sciences 2010 / p. 441-447 : ill

https://www.researchgate.net/publication/240613999_An_Approach_for_Verification_Assertions_Reuse_in_RTL_Test_Pattern_Generation

Constraint-based hierarchical untestability identification for synchronous sequential circuits

Raik, Jaan; Rannaste, Anna; Jenihhin, Maksim; Viilukas, Taavi; Ubar, Raimund-Johannes; Fujiwara, Hideo Sixteenth IEEE European Test Symposium : 23-27 May 2011, Trondheim 2011 / p. 147-152

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Viilukas, Taavi; Raik, Jaan; Ubar, Raimund-Johannes; Rannaste, Anna; Jenihhin, Maksim; Fujiwara, Hideo Info- ja kommunikatsioonitehnoloogia doktorikooli IKTDK viienda aastakonverentsi artiklite kogumik : 25.-26. novembril 2011, Nelijärve 2011 / p. 139-142 : ill

Identifying untestable faults in sequential circuits using test path constraints

Viilukas, Taavi; Karputkin, Anton; Raik, Jaan; Jenihhin, Maksim; Ubar, Raimund-Johannes; Fujiwara, Hideo Journal of electronic testing : theory and applications (JETTA) 2012 / p. 511-521 : ill <https://link.springer.com/article/10.1007/s10836-012-5312-5>

RT-level identification of potentially testable initialization faults

Raik, Jaan; Fujiwara, Hideo; **Krivenko, Anna** The Ninth IEEE Workshop on RTL and High Level Testing (WRTL 2008), Sapporo, Japan 2008 / [6] p https://www.researchgate.net/publication/234032548_RT-level_identification_of_potentially_testable_initialization_faults

Untestable fault identification in sequential circuits using model-checking

Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes; Krivenko, Anna** Proceedings of the 17th Asian Test Symposium ATS 2008 : November 24-27, 2008, Sapporo, Japan 2008 / p. 21-26 : ill <http://dx.doi.org/10.1109/ATS.2008.22>

Untestable fault identification in sequential circuits using model-checking

Raik, Jaan; Fujiwara, Hideo; **Ubar, Raimund-Johannes; Krivenko, Anna** 2002-2011 : 20th Anniversary compendium of papers from Asian Test Symposium 2011 / p. 257-262 : ill <https://ieeexplore.ieee.org/document/4711554>