

Automatic SoC level test path synthesis based on partial functional models

Tšertov, Anton; Ubar, Raimund-Johannes; Jutman, Artur; Devadze, Sergei 2011 Asian Test Symposium (ATS) : New Delhi, India 2011 / p. 532-538 <https://ieeexplore.ieee.org/document/6114730>

In-system programming of non-volatile memories on microprocessor-centric boards

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2014 / p. 25-34 : ill

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom Proceedings of the 20th International Conference Mixed Design of Integrated Circuits and Systems : MIXDES 2013, Gdynia, Poland, June 20-22, 2013 2013 / p. 408-413 : ill

On in-system programming of non-volatile memories

Tšertov, Anton; Devadze, Sergei; Jutman, Artur; Jasnetski, Artjom International journal of microelectronics and computer science 2013 / p. 72-78 : ill

Open-source JTAG simulator bundle for labs

Shibin, Konstantin; Devadze, Sergei; Rosin, Vjatšeslav; Jutman, Artur; Ubar, Raimund-Johannes International journal of electronics and telecommunications 2012 / p. 233-239 : ill <https://journals.pan.pl/Content/87192/PDF/32.pdf>

Trainer 1149: a boundary scan simulation bundle for labs

Jutman, Artur; Ubar, Raimund-Johannes; Devadze, Sergei; Shibin, Konstantin; Rosin, Vjatšeslav MIXDES 2011 : 18th International Conference "Mixed Design of Integrated Circuits and Systems" : June 16-18, 2011, Gliwice, Poland 2011 / p. 520-525