

Abstraction of clock interface for conversion of RTL VHDL to SystemC

Saif Abrar, Syed; Jenihhin, Maksim; Raik, Jaan 2014 IEEE International Advance Computing Conference (IACC) : February 21-22, 2014, Gurgaon, India 2014 / p. 50-55 : ill

Extensible open-source framework for translating RTL VHDL IP cores to SystemC

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FSMD RTL design manipulation for clock interface abstraction

Abrar, Syed Saif; Jenihhin, Maksim; Raik, Jaan 2015 International Conference on Advances in Computing, Communications and Informatics (ICACCI) : 10-13 August 2015, Kerala, India 2015 / p. 463-468 : ill <http://dx.doi.org/10.1109/ICACCI.2015.7275652>

Mutation analysis for systemC designs at TLM

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On the reuse of TLM mutation analysis at RTL

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Performance analysis of cosimulating processor core in VHDL and SystemC

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