

### **Diagnostic modeling of digital systems with multi-level decision diagrams**

**Ubar, Raimund-Johannes; Raik, Jaan; Jutman, Artur; Jenihhin, Maksim** Design and test technology for dependable systems-on-chip 2011 / p. 92-118 : ill [https://www.researchgate.net/publication/344994231\\_Diagnostic\\_Modeling\\_of\\_Digital\\_Systems\\_with\\_Multi-Level\\_Decision\\_Diagrams](https://www.researchgate.net/publication/344994231_Diagnostic_Modeling_of_Digital_Systems_with_Multi-Level_Decision_Diagrams)

### **High-level decision diagram simulation for diagnosis and soft-error analysis**

**Raik, Jaan; Repinski, Urmas; Jenihhin, Maksim; Chepurov, Anton** Design and test technology for dependable systems-on-chip 2011 / p. 294-309 : ill <https://www.igi-global.com/chapter/high-level-decision-diagram-simulation/51406>

### **High-speed logic level fault simulation**

**Ubar, Raimund-Johannes; Devadze, Sergei** Design and test technology for dependable systems-on-chip 2011 / p. 310-335 : ill <https://www.igi-global.com/chapter/high-speed-logic-level-fault/51407>

### **Preface**

**Ubar, Raimund-Johannes; Raik, Jaan; Vierhaus, Heinrich Theodor** Design and test technology for dependable systems-on-chip 2011 / p. xxii-xxviii

### **Sequential test set compaction in LFSR reseeding**

**Jutman, Artur; Aleksejev, Igor; Raik, Jaan** Design and test technology for dependable systems-on-chip 2011 / p. 476-493 : ill <https://ieeexplore.ieee.org/document/4738292>

### **System-level design of NoC-based dependable embedded systems**

**Tagel, Mihkel; Ellerjee, Peeter; Jervan, Gert** Design and test technology for dependable systems-on-chip 2011 / p. 1-36 : ill [https://pld.ttu.ee/~raiub/BOOK\\_content/Section\\_1/Ch11\\_jervan/Ch11\\_jervan\\_.pdf](https://pld.ttu.ee/~raiub/BOOK_content/Section_1/Ch11_jervan/Ch11_jervan_.pdf)